

VEDIC MULTIPLIER DESIGN AND POWER ANALYSIS

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Abstract: This paper demonstrates the capability of reducing power and area in CMOS VLSI blocks. The majority of power in CMOS devices is utilised during gate transitions. As a result, CMOS circuit control estimate is transformed into progress action estimation. Several approaches are used to simulate the evolution of CMOS circuits. The suggested Vedic multiplier is designed using multiple full adder cell techniques. The structure of complete adders for low power is obtained, and low power blocks are activated on the predetermined multiplier, with the results being broken down for better execution. The structures are completed using the TANNER S-EDIT tool and reproduced with T-SPICE.

Keywords : CMOS, Full Adder, Vedic multiplier, Low power, XOR, XNOR, MUX.

I. INTRODUCTION

"Very Large Scale Integration" is the technical term for VLSI. An breakthrough known as VLSI (very enormous scale-coordination) allows the fabrication and integration of large numbers of transistors (millions) on one integrated circuit. At least one entrance is included in a coordinated circuit, which is built on a single silicon chip. Because of the complexity of today's VLSI design and implementation, a manual approach is no longer an option. With the rapid advancements in mechanical technology, structure robotization has become a pressing need. [5]. The low power VLSI structure problem understands how much demanded it will be into two exams with improvement in the general public at large generally. Problems arise when trying to estimate the power or vitality dispersion throughout the course of the planning process with any accuracy. The methods of research differ greatly in terms of accuracy and efficiency. In addition, the examination approach serves as the starting point for simplifying the plan. [3] The ability of integrated circuits to evolve to new levels necessitates the development of low-power VLSI devices. The growing need for battery-operated client gear is one factor driving the demand for low-power CPUs forward. Natural concerns are also a major factor in the need for low-power chips and frameworks. The rigour and efficiency of the two approaches of testing are diametrically opposed.

II. DESIGN OF FULL ADDERS

A. Most mathematical operations begin with the addition of binary zeros and ones. One of its most important functions is to do basic multiplication and division operations as well as to calculate the addresses of all the memory locations that may be accessed. As a result, their speed enhancement has the potential for a wide range of improved applications. Depending on the application and low power consumption, many adder designs may be employed. Signed multipliers have power decreases that are explored in this research, as are comparisons of the power of various multipliers. The 10T full adder was switched out for an 8T full adder to reduce power consumption. The PTL-dependent circuits, on the other hand, are unquestionably useful in building larger circuits, such as different section input adders and multipliers. In this study, an 8-transistor 8T full adder is shown to have a high failure power and a quick full adder cell. Five complete adder cells are used to test the new structure's capabilities, and their performance is compared to that of the old one in several ways, such as control use and deferral.

B. XOR Full Adder Design

Every sophisticated circuit needs a Full Adder to function properly. The appearance of a large VLSI circuit may be dramatically altered by a simple adjustment in transistor check, power, and postpone [6]. The display of multipliers is dependent on the use of the whole adder. To conduct the examinations, we make use of the specialised full adders. The first is a 10T XOR full adder, which uses four transistor XOR gates in its construction to implement the ten transistor full adder shown in Figure 1. Figure 5 shows a schematic for the XOR complete adder with eight transistors that we've suggested. The smallest amount of silicon area is obtained by relying on three transistor XOR gates. 3T XOR gate schematic is shown in Figure (2).

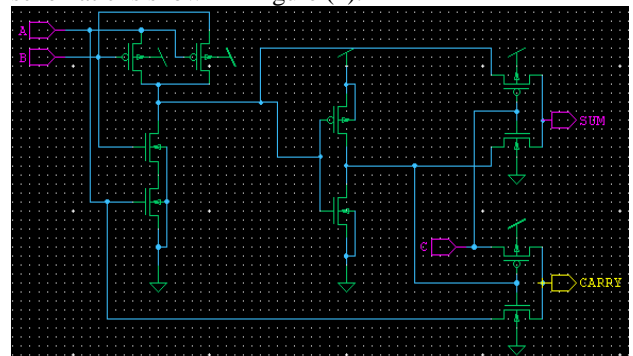


Fig. 1. 10T XOR adder

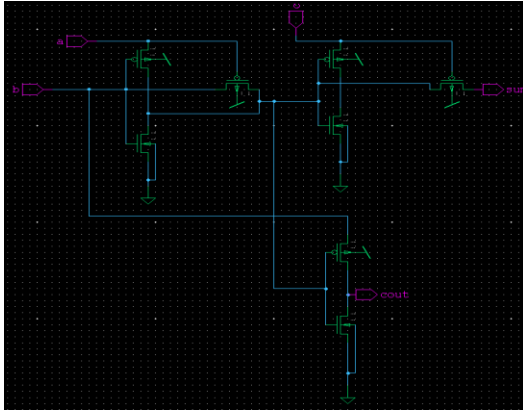


Fig. 2. 8T XOR adder

C. XOR Full Adder Design

It is the 10T full adder, which is an XNOR full adder, that uses pass transistor logic (PTL) for the second full adder. In figure plan [9], a full adder with 4T XNOR is referred to as a static vitality recuperation full adder. The disposal of the path in the direction of the location reduces the absolute power consumption by reducing the tiny out power consumption.

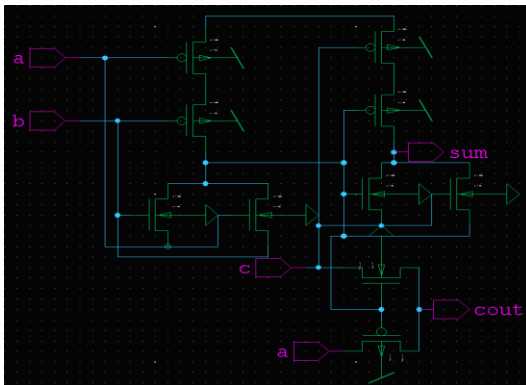


Fig 3. 10T XNOR adder

There are two XNORs and a single mux in the static energy recovery full adder shown in the image. The four-transistor XNOR was shown in the illustration (3). The XNOR 8T complete adder, shown in figure (4), is based on a 3 transistor XOR gate and gains the lowest amount of silicon space. 3T XOR gate schematic is shown in Figure (4).

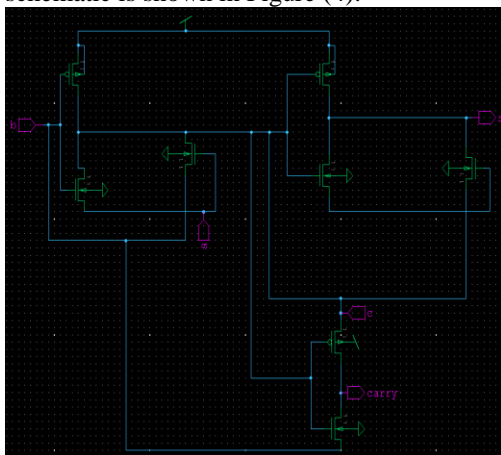


Fig. 4. 8T XOR adder

D. Design of Full Adder using 2:1 MUX

Third-generation complete adder circuits include a 2:1 multiplexer circuit and two inverters. The system's goal is to avoid several transmission chain limit voltage mishaps by legitimately reestablishing system dimensions. The CLRL adder has a single edge voltage imbalance problem, which requires the base voltage, according to DC and transient analysis.

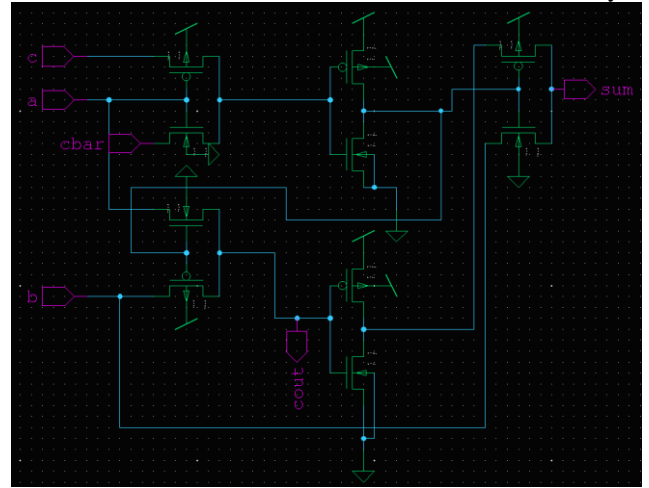


Fig. 5. 10 Transistor adder using 2:1 MUX

Complimentary and Level-Restoring is the third kind of suggested setup Figure 1 shows the carry logic adder, which consists of a 2:1 multiplexer circuit and an inverter (6). It has a capacity of only 8 litres. The strategy is to avoid multiple edge voltage disasters in the convey chain by reestablishing the right dimensions.

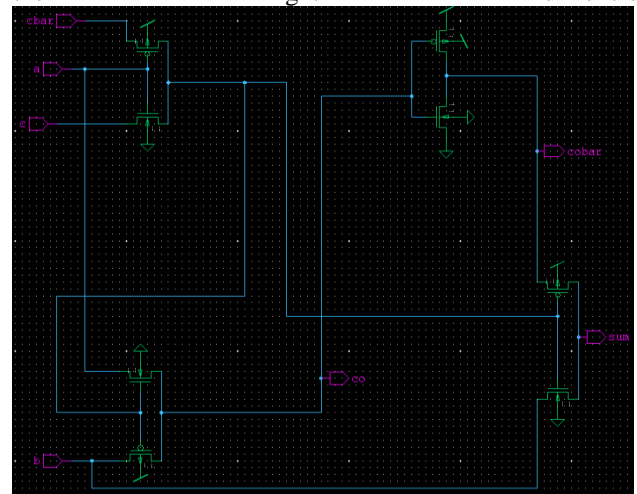


Fig 6. 8T Full adder using 2:1 MUX

E. Shannon Full Adder Design

Capacity inputs are connected to the control input terminals. Table I's inner yield from the SUM circuitry is used as input to the carry logic instead of all the contributions from the outside information in the suggested adder 2 [8]. A pass transistor logic 8T transistor full adder is used. Shannon's full-adder circuit, as seen in this image (8). A signal circuit multiplexes the total and convey activity [11].

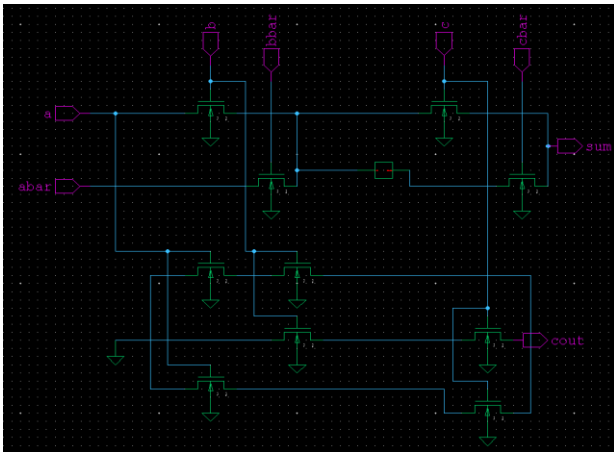


Fig. 7. 12T Shannon full adder

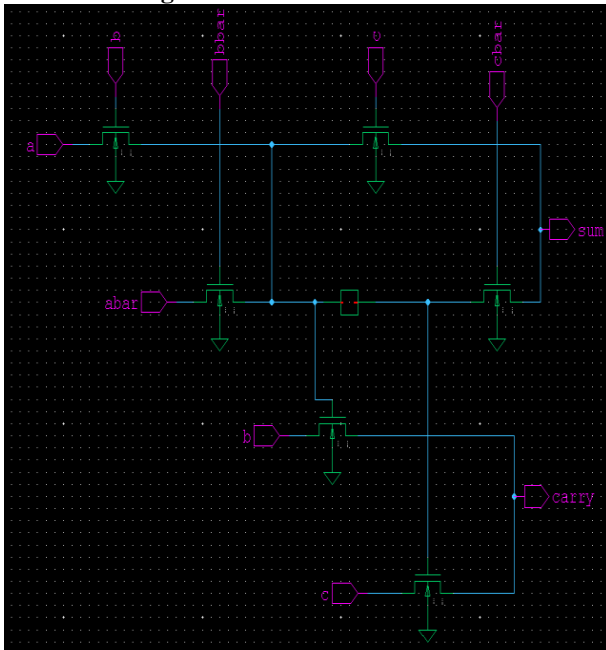


Fig. 8: 8T Shannon full adder

III. FULL ADDER RESULT AND DISCUSSION

In terms of execution contrast, the new 8T full adders outperform all other full adders. Look at a 10T complete adder for a reduced transistor test and reduced power consumption. The vast majority of adders use the same input sources and outputs. Inputs for all adders are as follows:

A=1001, B=1011, C=0111

Outputs: SUM=0101, CARRY=1011

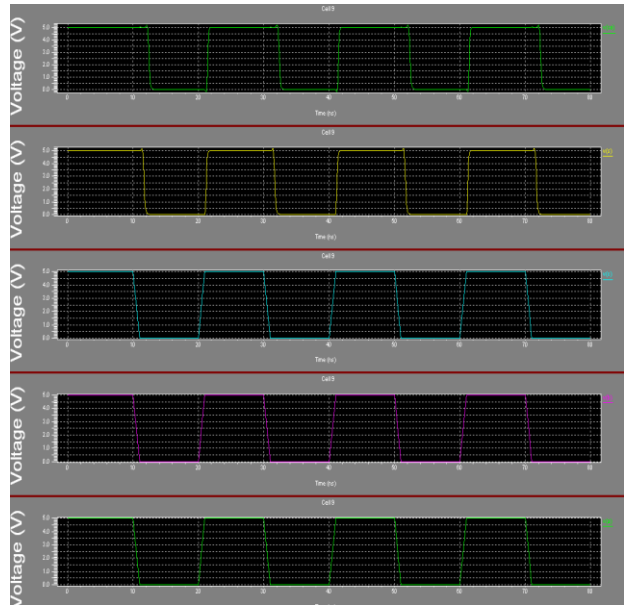


Fig. 9. 12T Full adder output waveform

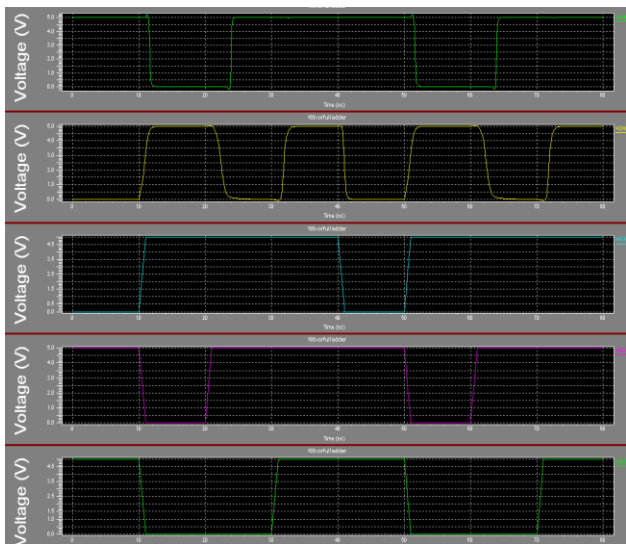


Fig. 10. 10T Full adder output waveform

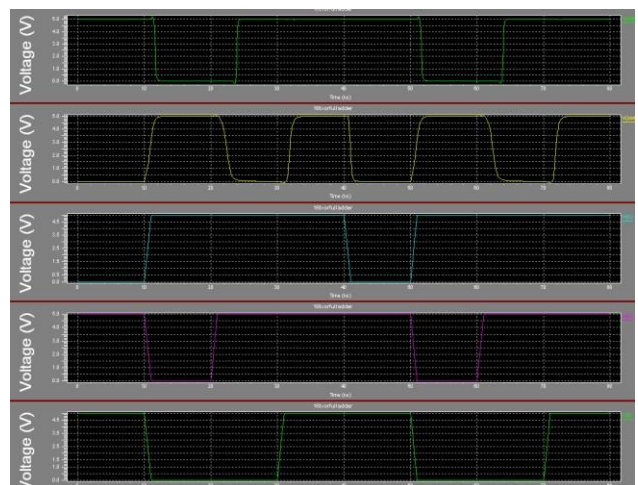


Fig. 11. 8T Full adder output waveform

Table I: Comparisons of Full Adders

Full Adder Type	Power(watts)		Transistor count	
	Existing method	Proposed method	Existing method	Proposed method
XOR	0.146	0.094	10	8
XNOR	0.125	0.082	10	8
CLRCL	0.112	0.071	10	8
SHANNON	0.102	0.058	12	8

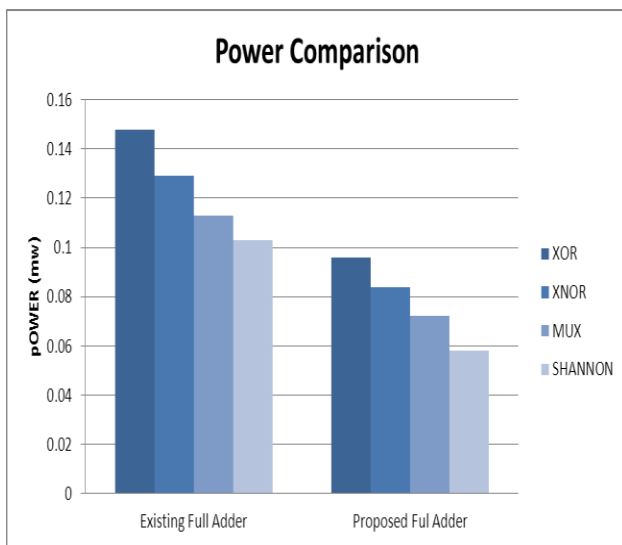


Fig. 12. Power comparison of Full Adders

IV. DESIGN OF VEDIC MULTIPLIER

Figure 13 [2] shows the typical implementation of a 4x4 bit Vedic multiplier module using four 2x2 bit Vedic multiplier modules and a 10T and 12T full adder module. Four 2x2 bit Vedic multiplier modules [1] and 10T and 12T complete adder modules [2] are used in the proposed design of a 4x4 piece Vedic multiplier module, as shown in figure 13.

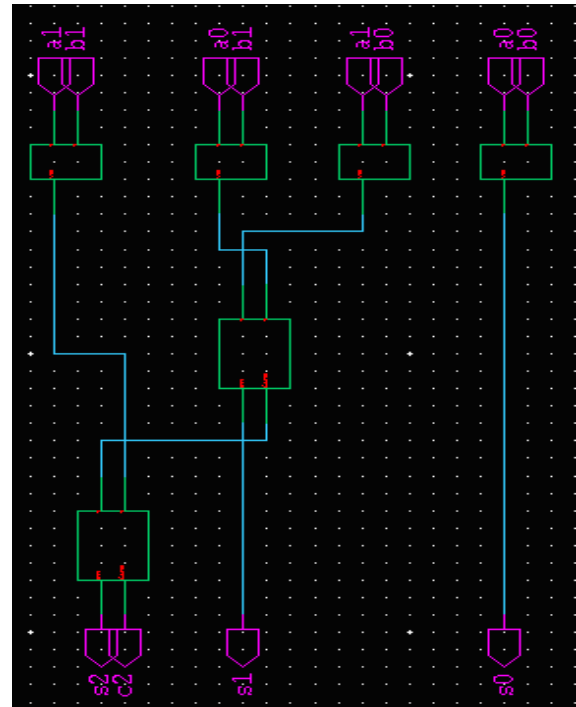


Fig. 13. Conventional Vedic Multiplier (2x2)

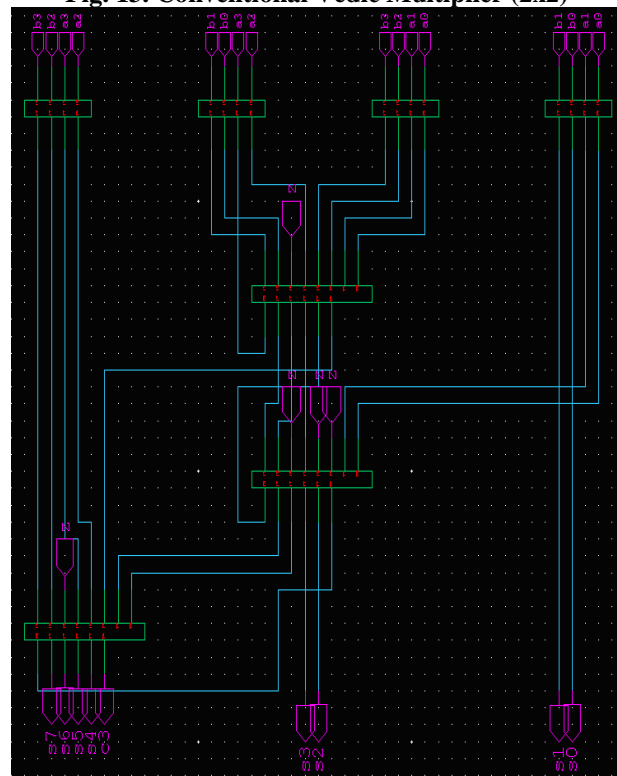


Fig. 14. Conventional Vedic Multiplier (4x4)

Different adder units are used to compare the multiplicative power of various multipliers. Figure shows a power comparison between several full adders. Moreover, the power outputs show that the Shannon full adder uses less power than any other adder [3].

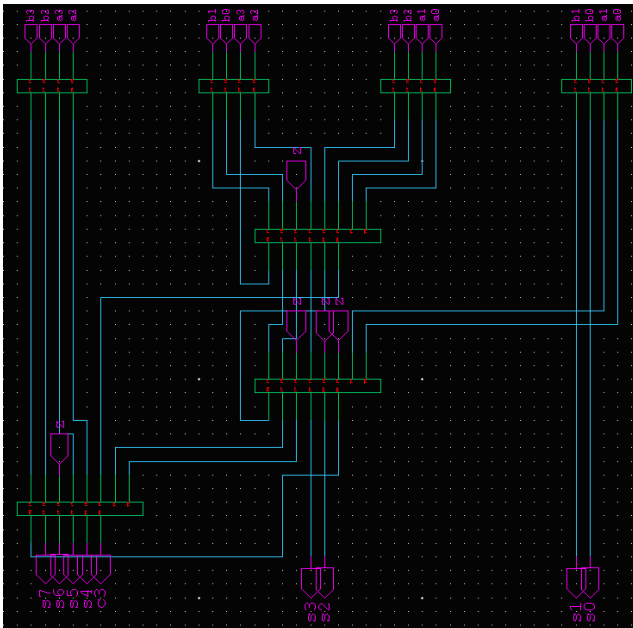


Fig. 15. Proposed Vedic Multiplier (4x4)

The power findings and a comparison graph are provided in figure for the current and suggested multipliers, which are each developed using a different full adder (18). They vary in transistor count because of the different components that make up the multiplier. Multiplier transistor count findings are shown in the table below (2)

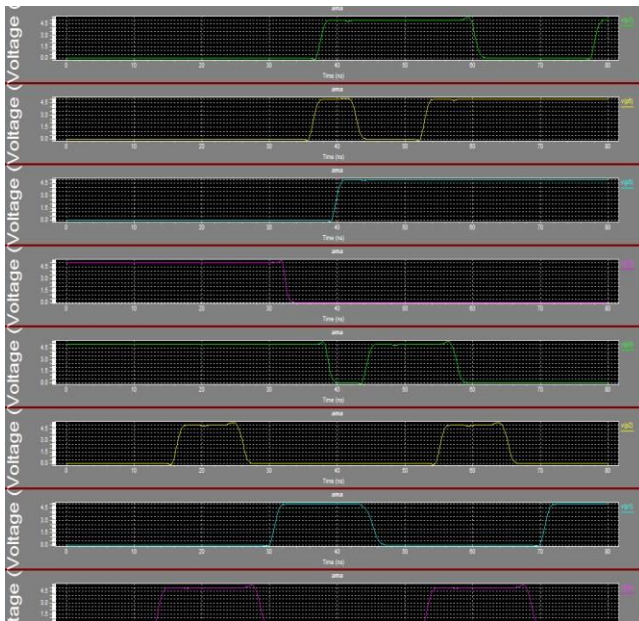


Fig. 16: Conventional Multiplier output waveform

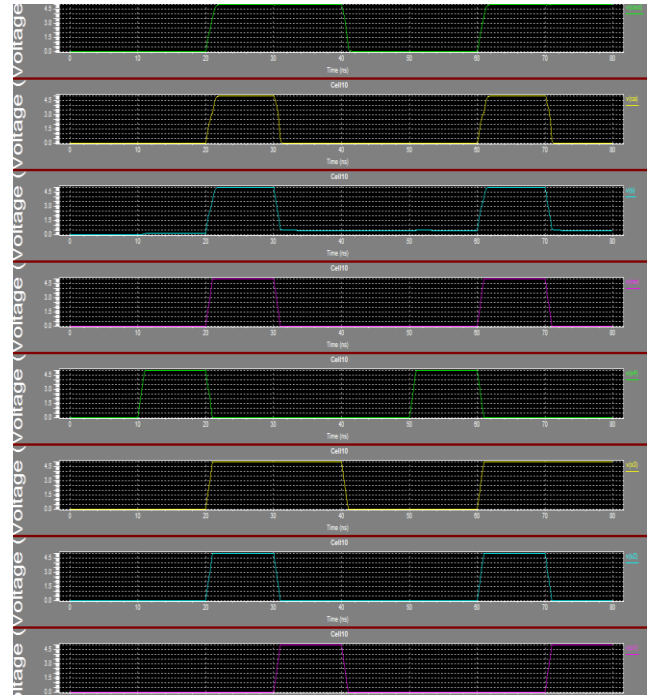


Fig. 17. Proposed Multiplier output waveform

The suggested multiplier using Shannon's complete adder may be found to be more power-efficient, and it has an exceptionally low transistor count, as seen in the preceding results.

Table II: Comparisons of Different Types of Multipliers

Multiplier Type	Adder type	Power (mw)		Transistor count	
		Existing method	Proposed method	Existing method	Proposed method
Vedic multiplier	XOR	10.04	9.08	212	188
	XNOR	9.01	8.12	212	188
	CLRCL	8.25	7.43	212	188
	SHAN NON	7.53	6.85	234	188

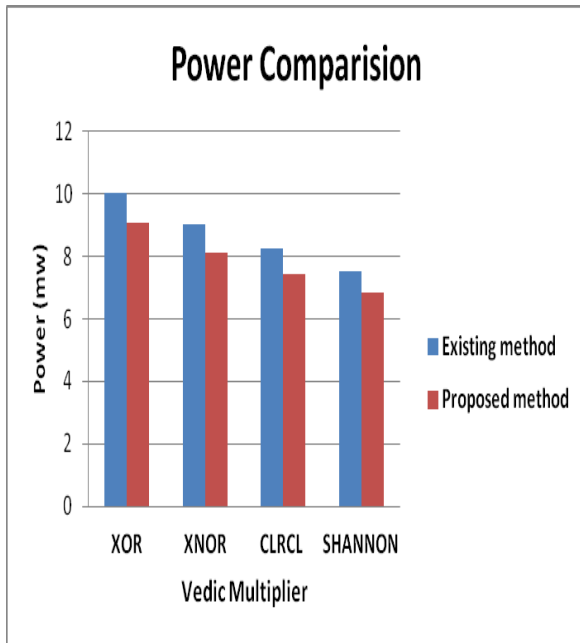


Fig. 18. Power comparison of Multipliers

V. CONCLUSION

Eight-transistor full adders use 30 percent less power and have 36 percent more control reserve funds compared to the traditional 12-transistor full adders. Comparing the 8T full and its companions, the least delay is present in the future. Four different complete adders were used to construct four different multipliers, and their display was studied. In every scenario, the Proposed 8T full viper multipliers have the lowest power deferring item. The proposed CMOS full adder multipliers feature an 8.6% decrease in transistor count and a 10.4% reduction in power compared to the current CMOS full adder multipliers. Full adder 10T multipliers feature 13.12 percent more transistors and a 17.4 percent power decrease compared to their predecessors, which had a 13.12 percent transistor count. There are also 17.9 percent fewer transistors in the proposed multipliers with 8T compared to the present multipliers, and 8.6 percent less power.

REFERENCES

1. P.Sakthi, S.Maheswari, P.Yuvarani, "High Performance Vedic Multiplier using Compressors", International Journal of Applied Engineering Research, ISSN 0973-4562 Vol. 10 No.20 (2015), pages 16882-16886.
2. P.Sakthi, P.Yuvarani, "Multipliers based on Urdhva Tiryagbhyam Algorithm: A Survey", Advances in Natural and Applied Sciences, ISSN:1995-0772, 8(19) Special 2014, Pages: 100-106.
3. S. Kiruthika, R.Nirmal Kumar, Dr. S.Valarmathy, Issue 1, January 2013, "Comparative Analysis of 4bit Multipliers Using Low power 8-Transistor Full Adder cells" International Journal of Emerging Technology and Advanced Engineering (IJETA) Volume 3, ISSN 2250-2459, ISO 9001:2008.
4. Siddharth S.G, Ramkumar M, Kiruthika.S, 2014, "Railway Track Scanning and Surveillance Robot Using Wireless Technology" Journal of Harmonized Research in Engineering (JOHR) Volume 2, Issue 1, 2014, (pp194-200).
5. S.Kiruthika, A.Vimala Starbino, "Design and analysis of FIR filters using low power multiplier and full adder cells", IEEE 2017.
6. S.Kiruthika, B.Balraj, "Design of Wallace tree multiplier based on 0.12 μ m CMOS technology using GDI full adder".2018, International Journal of pure and applied mathematics Volume 119, Special Issue.

7. J. Wang, S. Fang, and W. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," IEEE J.Solid-State Circuits, vol.29, no. 7, pp. 780-786, Jul. 1994.
8. Karunakaran P, S. Venkatraman, I.Hameem Shanavas, and T. Kapilachander. "Power Optimized Multiplier Using Shannon Based Multiplexing Logic", International Journal of Intelligent Systems and Applications, 2012.
9. Deepa, Sampath KumarV, "Analysis of Low Power 1-bit Adder Cells Using Different XORXNOR Gates", 2015 IEEE International Conference on Computational Intelligence & Communication Technology, 2015.
10. "Neuronal Logic gates realization using Vedic mathematics", 2015 1st International Conference on Next Generation Computing Technologies (NGCT), 2015
11. P. Yuvarani, 2012, 'Image denoising and enhancement for lung cancer detection using soft computing technique,' IET Chennai 3rd International on Sustainable Energy and Intelligent Systems (SEISCON 2012), pp. 1-4.