

Design and Implementation of 5G LDPC Decoder Architecture with Parallel and Adaptable on FPGA Target

Mr. M. Ramana Reddy⁽¹⁾ Mr. B. Ajantha Reddy⁽²⁾ Kalle Bhavani⁽³⁾ Kalle Bhavani⁽⁴⁾ Kalle Bhavani⁽⁵⁾ Kalle Bhavani⁽⁶⁾

^{1,2} Krishna Chaithanya Institute Of Technology & Sciences, Ece Department, Markapur, Andhra Pradesh.

^{3,4,5,6} Krishna Chaithanya Institute Of Technology & Sciences, UG Student-ECE, Markapur, Andhra Pradesh.

Abstract. The article presents we implement for the fifth generation (5G) cellular network technology, a crucial error correcting code is the quasi-cyclic (QC) low-density parity-check (LDPC) code. The 5G LDPC coding structure is intended to accommodate several frame sizes and code speeds enables great parallelism to achieve 10 Gb/s, a highly demanding data rate. The hardware design is put under difficult constraints by this remarkable performance. Processing rate penalties may be introduced on some configurations if such high flexibility is allowed. Field-programmable gate array (FPGA) devices are the focus of a unique, highly parallel, and flexible hardware design for the 5G LDPC decoder that is suggested in this context. To maximize the utilization of the processing units and greatly increase the processing rate, the architecture offers frame parallelism. The controller unit was meticulously engineered to prevent update conflicts and support all 5G configurations. Additionally, a productive data scheduling strategy is suggested to boost the processing rate. For many setups, the suggested FPGA prototype outperforms the latest related state of the art in terms of processing rate per hardware resource.

Keywords: LDPC(Low Density Parity Check),5G Communications, FPGA, Verilog HDL, Variable Node Unit(VNU)and Check Node Unit(CNU).

I.INTRODUCTION

It is anticipated that future communication systems will offer several services, each with unique system settings tailored for needs, like latency, data rate as well as energy usage. The quasi-cyclic (QC) low-density parity-check (LDPC) code [1] has been chosen as the next error correction code for the next fifth generation (5G) communication systems [2] to achieve these demanding specifications. Multiple frame sizes can be supported at a granularity level of a few bits for multiple code rates ranging from 1/5 to 9/10 thanks to the 5G LDPC code architecture. In addition, the 5G LDPC code's base graphs can be stretched up to 384 times, supporting extremely high parallelism levels to ensure the anticipated 10 Gb/s data flow in 5G networks [3]. At the base station, field programmable gate arrays (FPGAs) can incorporate the 5G LDPC decoders. Because these devices are reprogrammable, the physical layer can be changed to reflect how the upcoming standards will develop in the future, which will save money for the telecom operators. Consequently, there's a lot of interest in creating 5G LDPC. devices with FPGA decoders. All of the 5G features, however, place strict limitations on hardware design; the architecture needs to be thoughtfully created to accommodate every possible 5G configuration. Additionally, the code

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structure of the 5G LDPC is optimized to facilitate high parallelism, but exclusively for lengthy frames that employ the largest lifting sizes. The most current cutting-edge 5G LDPC decoder architectures [5]– [7] overlook this problem. Ultimately, the complexity of the permutation network is higher than that of a barrel shifter as it is currently implemented in a standard LDPC and problems with routing. This research proposes a novel hardware architecture for a 5G QC-LDPC decoder that targets FPGA devices in order to address these problems. The architecture has great adaptability and a rapid rate of processing across all frame sizes. It is suggested that frame parallelism be used to decode small frame sizes to maximize the use of hardware resources and processing power [8]. The usage of a low complexity permutation network that has recently been suggested in the literature [9], [10], makes this practicable. To decrease the quantity of update conflict during decoding and raise processing rate, effective data scheduling is also used. Furthermore, an appropriate quantization technique is provided for 5G QC-LDPC decoders after a thorough analysis of the quantization process.

This code design permits high parallelism levels for great processing throughput and appropriate hardware implementation. Nonetheless, in contrast to current code designs in other standards, the 5G QC-LDPC encoder and decoder must accommodate several lifting sizes Z and BGs. The symbols n_{cb} , n_{rb} , and n_{eb} stand for the number of columns, rows, and edges of the BG number b , respectively. $d_{ci,b}$ is the CN degree at row i and BG b . On the other hand, $d_{vi,b}$ represents the VN degree at column j and BG b . The degrees of the check node (CN) and variable node (VN) are seen to be significantly unequal at various rows and columns. The 5G QC-LDPC coding is hence erratic. Moreover, not all of the rows have row-by-row orthogonality guaranteed, which may result in update conflicts in a real-world implementation. This article aims to bridge the gap between theoretical analyses and practical implementations by incorporating both theoretical insights and real-world implementation results. By considering factors beyond idealized scenarios, such as hardware constraints and buffer insertion, a more comprehensive understanding of the multiplier's performance and effectiveness can be achieved.

A. 5G LDPC Code Structure

II.EXISTING SYSTEM

This Method is A new QC-LDPC code is used as a data channel coding system for 5G communications. The base-graph (BG), or prototype matrix, serves as the foundation for code development. This BG's nonnull elements are each extended by a Z -by- Z identity matrix that has been circularly moved, with Z standing for lifting size. The Z and edge positions in the BG determine the values of the circular shift (rotation).

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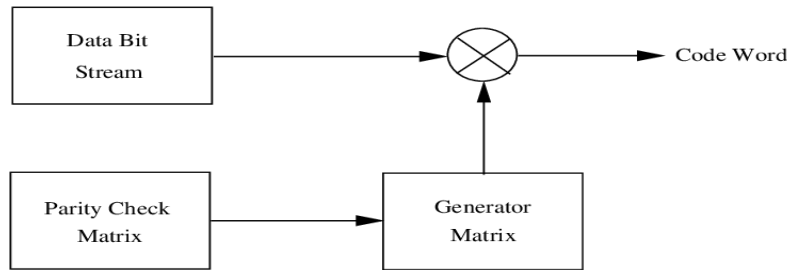


Figure.1 LDPC Encoder Block diagram

B. Layered Decoding Algorithms

As the conventional multiplication method may not be the most efficient, following message encoding and transmission across the noisy channel, the channel LLRs L_i that feed the LDPC decoder are represented as $L_i = 2y_i/\sigma^2$,

where y_i is the signal received. Moreover, we have $y_i = x_i + w_i$, where w_i is the variance σ^2 additive Gaussian noise term and x_i is the i th transmitted modulated symbol.

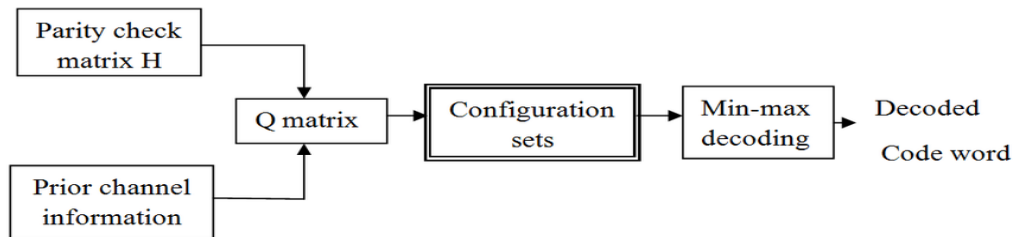


Figure.2 LDPC decoder Block diagram

The Low-Density Parity-Check (LDPC) system is a robust and efficient framework for achieving reliable communication over noisy channels. At its core, the LDPC system consists of encoding and decoding

modules, each designed to handle the transmission and reception of data efficiently while mitigating errors introduced by noise and interference.

C. Proposed LDPC Decoder

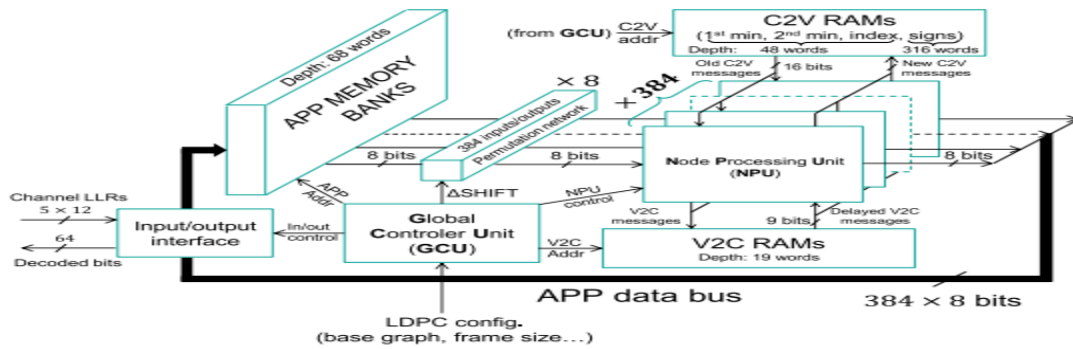
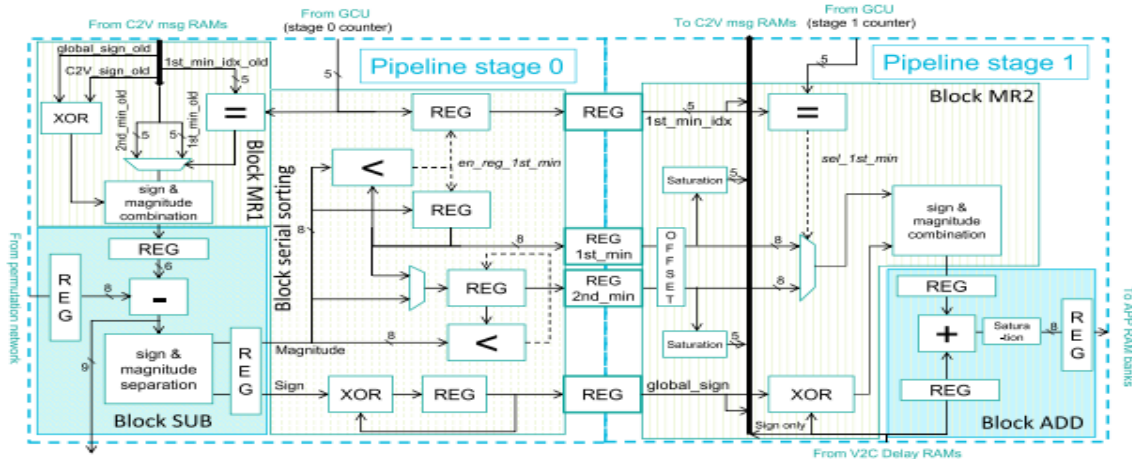


Fig.c. Proposed hardware architecture of the LDPC decoder.



Proposed hardware architecture NPU

LDPC encoding begins with the generation of a sparse parity-check matrix, typically represented in a structured form to facilitate efficient encoding operations.

The input data stream is divided into blocks, which are then mapped onto the rows of the parity-check matrix.

Each row of the matrix represents a parity-check equation, imposing constraints on the transmitted codeword. Through matrix multiplication or equivalent operations, the encoder generates the codeword by satisfying the parity-check equations, ensuring redundancy for error detection and correction

III. PROPOSED LDPC DECODER

This project proposes a new 5G LDPC decoder design for FPGA devices. High processing throughput and great flexibility are properties of the proposed decoder that support all 5G setups. The majority of the 384 parallel processing units can be repurposed to boost processing speed when using frame-level parallelism to handle small frame sizes throughput. According to synthesis results, at high code rates the suggested decoder performs better than the state-of-the-art decoders in terms of average processing throughput per LUT and FF, while maintaining competitiveness at low code rates. Based on post P&R synthesis results, the suggested architecture outperforms the recently released commercial Xilinx 5G LDPC decoder in

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terms of average processing throughput at the same complexity level.

Implementing a Low-Density Parity-Check (LDPC) decoder on an FPGA (Field-Programmable Gate Array) involves designing a hardware architecture that efficiently performs the decoding process. LDPC decoders are used in various communication systems, including those conforming to 5G standards. The operation on an FPGA involves parallel processing and efficient memory management. Below are the key steps involved in implementing an LDPC decoder on an FPGA. Fig. e. DFG for six-input LUT-based FPGA implementation of (a) 2- and (b) 4-bit binary polynomial multipliers. The FPGA implementation of all techniques for 2- and 8-bit multipliers is the same, regardless of the various DFGs. It is important to remember that the real architecture and routing are more intricate than this straightforward presentation.

The proposed architecture, shown in Fig. 3, contains a dual port APP memory bank which can store up to $n_{c1} = 68$ words of $Q_{APP} \times Z_{max} = 3072$ bits, where Q_{APP} corresponds to the number of bits for the APP. Based on a quantization study, it is set to 8 bits in our architecture. An input-output interface unit drives and writes the channel LLR into the APP memory bank and reads the decoded bits when the last iteration is reached. The addresses of the memory bank

correspond to the column indexes of the BG. A permutation network rotates Z outputs of the APP memory banks at each clock cycle. It is configured to support all rotation values from the 51 lifting sizes. The Z rotated APPs are then processed by up to $Z_{max} = 384$ node-processing unit (NPU) in parallel, enabling high-processing throughput. The NPU serially processes all the edges of the chosen BG. The C2V and V2C messages are updated and accessed through dedicated dual port RAMs connected to the NPUs. These RAMs are dimensioned as follows

1) The maximum number of V2C messages to store corresponds to the highest CN degree (d_{cmax}) among all rows and BGs: $d_{cmax} = \max_i, b(d_{ci}, b)$. Therefore, the V2C RAMs must be able to store a total of 19 words of $(Q_{APP} + 1) \times Z_{max} = 3456$ bits. 2) The C2V RAMs memorize the global messages (global signs, first minimum index, first, and second minimum

values) requires $\max_b(n_{rb}) = 46$ words of $Z_{max} \times (2^{(QC2V-1)} + \frac{1}{\log_2 d_{cmax}}) = 16 \times 384$ bits. The $QC2V$ parameter corresponds to the number of quantization bits used for the C2V messages including the sign bit, and is set to 6 in the proposed architecture. The addresses correspond to the row indexes.

3) The C2V sign messages are stored into RAMs containing a total of $\max_b(n_{eb}) = 316$ words of $Z_{max} = 384$ bits. The addresses correspond to the edge indexes

IV. RESULTS AND ANALYSIS DISCUSSION

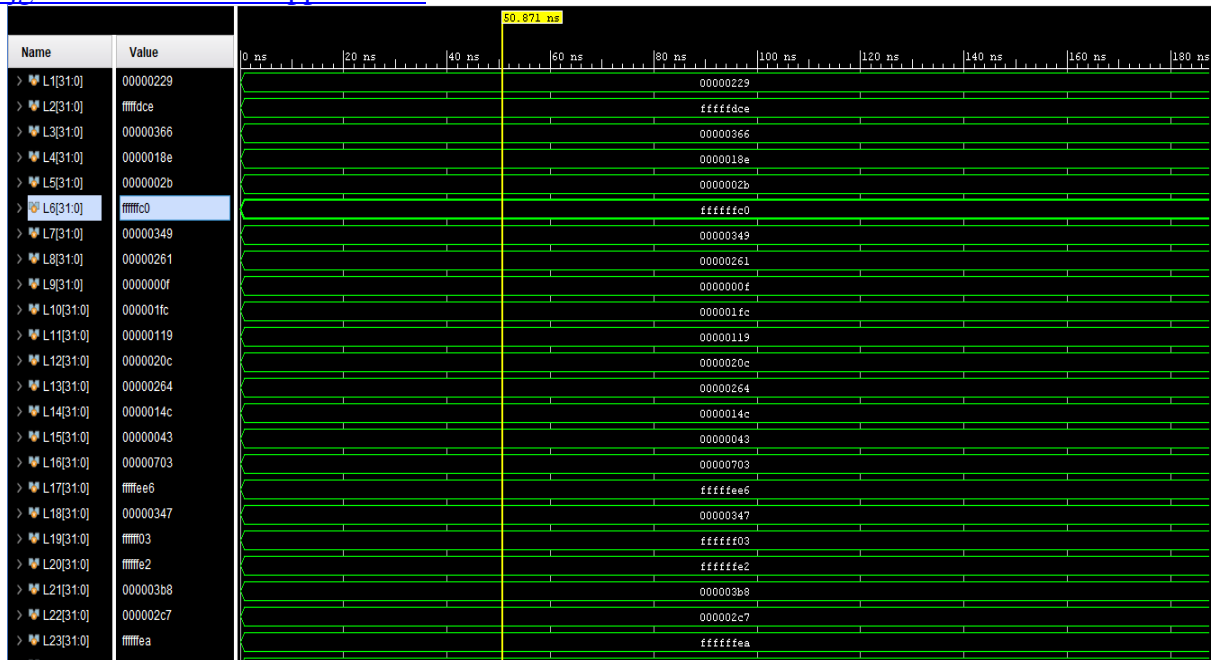


Fig.4 ldpc output.

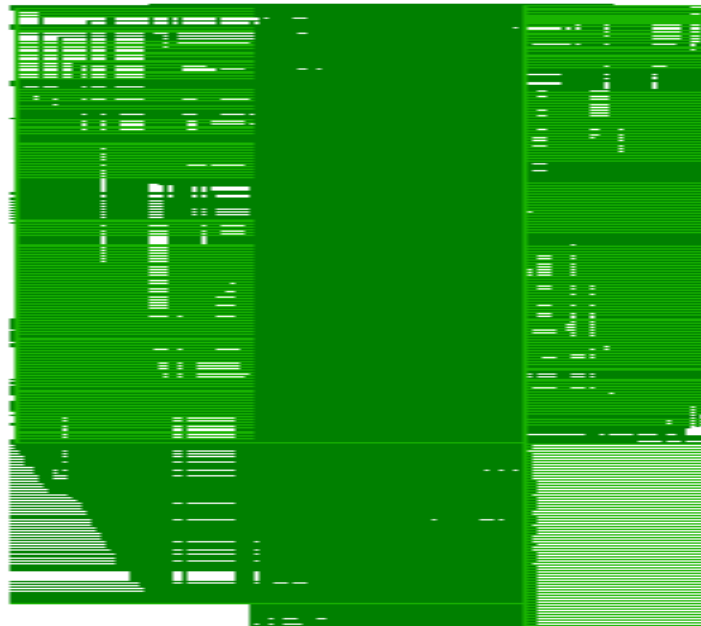


Fig.5.RTL schematic diagram.

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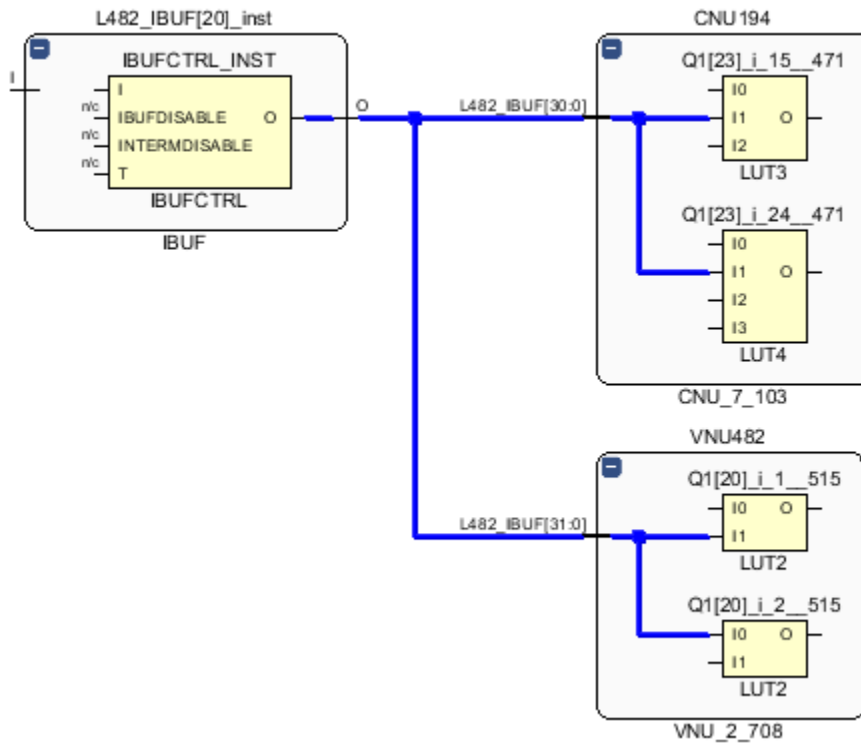


fig.6.LDPC Synthesis design

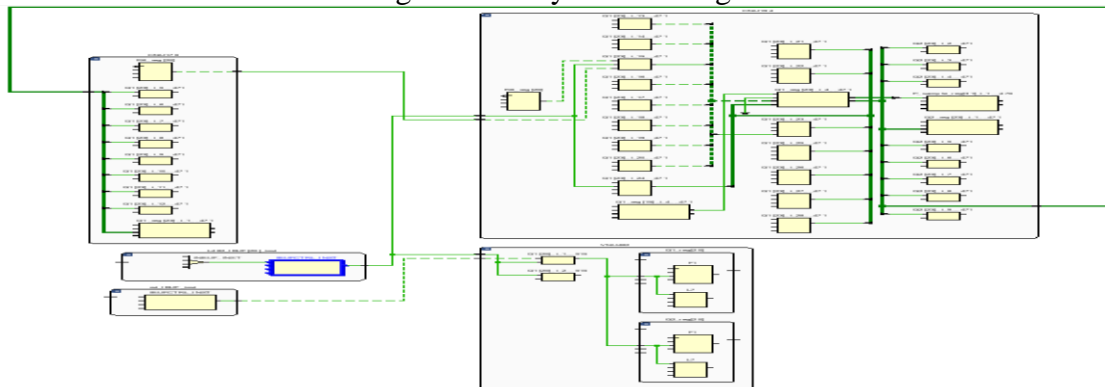


Fig.7.CNU synthesis design

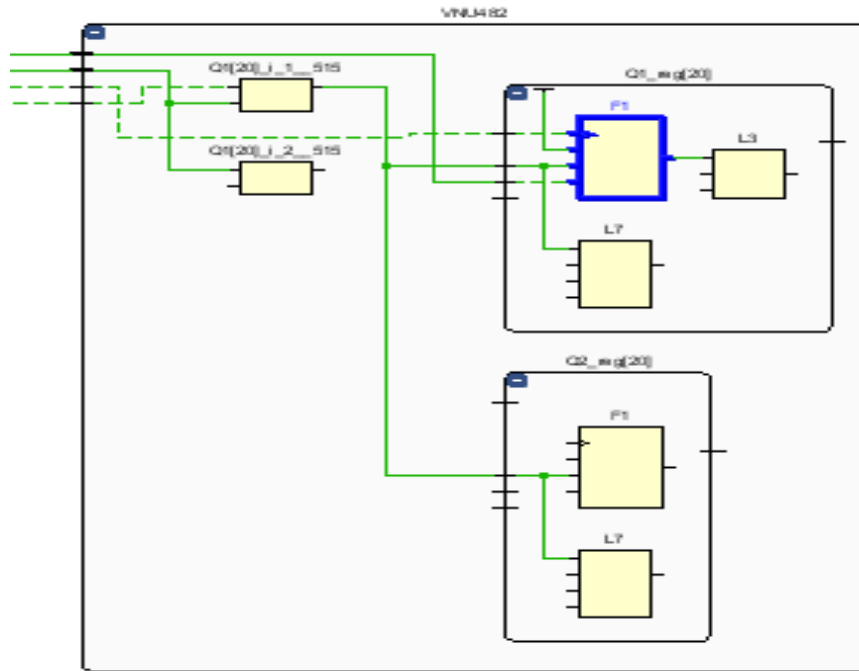


Fig.8.VNU synthesis

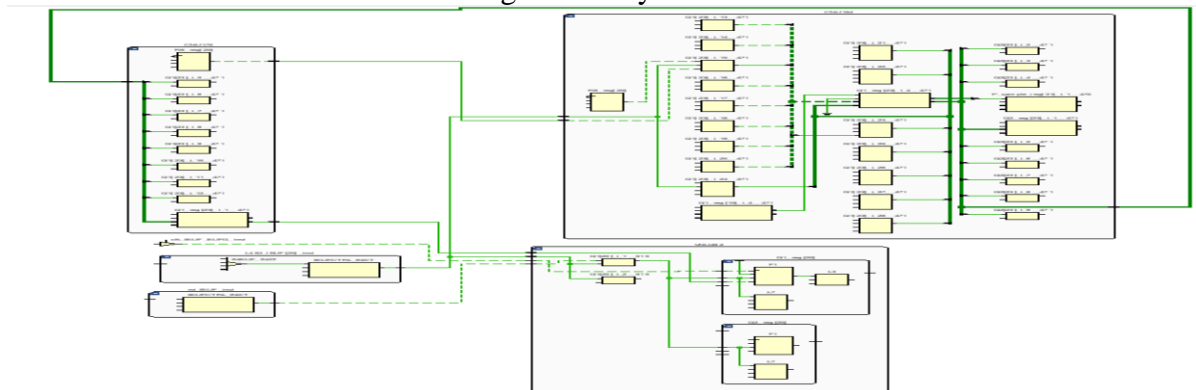


Fig.9.complete synthesis design of Idpc

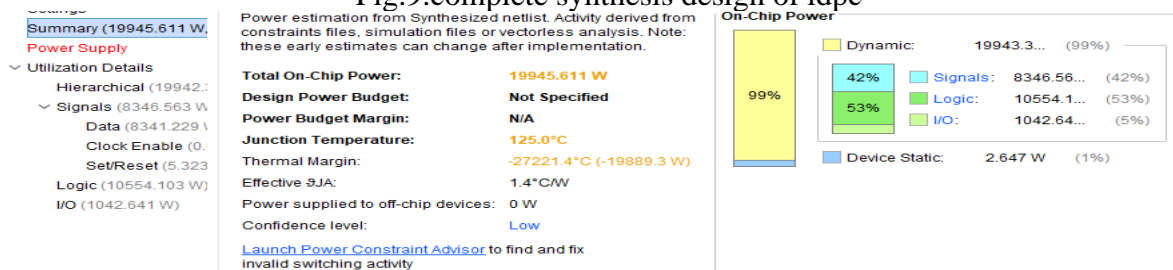
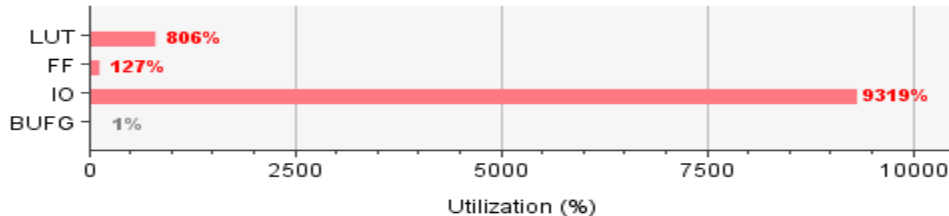
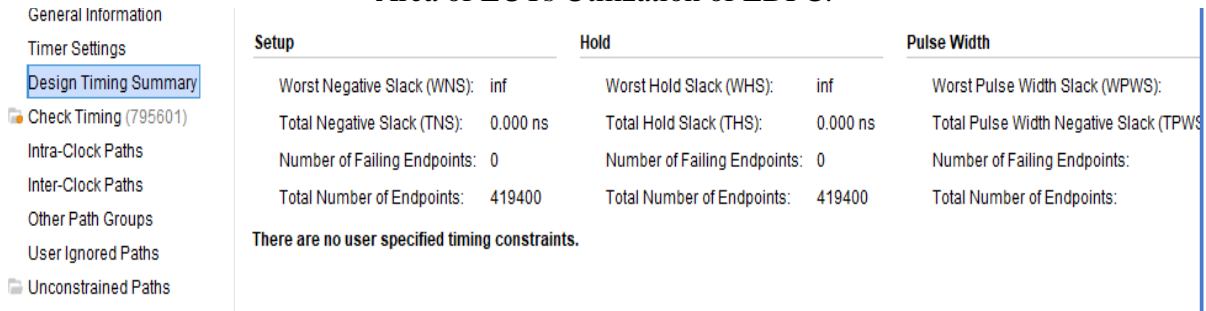


Fig10 power report

| Resource | Utilization | Available | Utilization % |
|----------|-------------|-----------|---------------|
| LUT | 943436 | 117120 | 805.53 |
| FF | 297168 | 234240 | 126.86 |
| IO | 19010 | 204 | 9318.63 |
| BUFG | 1 | 352 | 0.28 |



Area of LUTs Utilization of LDPC.



Timing report.

Fig.g. Simulation result of Karatsuba Multiplier.

CONCLUSION

A novel 5G LDPC decoder design for FPGA devices is proposed in this article. The designed decoder features high-processing throughput and high flexibility to support all 5G configurations. Thanks to the use of frame-level parallelism when short frame sizes are processed, most of the 384 parallel processing units can be reused to increase the processing throughput. Synthesis results show that the proposed decoder outperforms state-of-the-art decoders in terms of average processing throughput per LUT and FF for high code rates such as 0.815, while remaining competitive for low code rates. When compared with the recent commercial Xilinx 5G LDPC decoder, post P&R synthesis results show that the proposed

architecture provides higher average processing throughput while being less complex.

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