Accelerating and Improving Wafer Defect Classification based via Data-Centric Deep Optimized Learning

Mrs. k. Nandini[1], Bejjanki Venkata Rao[2], Dokku Yaswanth[3], Darla Indravathi[4], Gajula Ajay Kumar[5]
UG Scholar [2,3,4,5], Assistant professor [1],
Department. of CSE,
Seshadri Rao Gudlavalleru Engineering College,
Gudlavalleru Andhra Pradesh–521356, India
kagita.nandini@gmail.com[1] , bejjankivenkat8688@gmail.com[2] , lovelyyash555@gmail.com[3],
indravathidarla@gmail.com[4] ,ajaykumargajula79@gmail.com[5]

ABSTRACT

This research introduces a cutting-edge methodology to revolutionize the classification of wafer defects in semiconductor manufacturing. The study, driven by the imperative to enhance semiconductor technology, employs laser beam scattering experiments on silicon wafers. Integrating rapid object classification and dimensional reduction, our approach demonstrates remarkable efficiency when applied to real-world chip fabrication data. The fusion of deep learning techniques with thresholding and similarity measures enhances the precision of defect identification, overcoming challenges posed by complex geometries. Notably, our method exhibits a proclivity for low-dimensional search spaces, ensuring both rapid and quasi-linear predictions for real-world wafer data. Leveraging a dataset comprising 811,457 wafer maps from 46,393 lots in real-world fabrication, our research significantly contributes to automated failure pattern recognition. The meticulous analysis of various defect types, including Center, Donut, Edge-Loc, Edge-Ring, Loc, Random, Scratch, Near-full, and none, promises to elevate semiconductor yield through the identification of failure patterns at an early stage of fabrication.

Keywords: semiconductor technology, wafer defect classification, deep learning, efficiency, failure pattern recognition, paradigm shift, rapid object classification, dimensional reduction, complex geometries.

INTRODUCTION

The semiconductor industry stands at the forefront of technological innovation, and the continuous pursuit of enhanced performance and reliability necessitates advancements in defect classification on silicon wafers. Precise modeling of light scattering from nanometer-scale defects is crucial for pushing the boundaries of semiconductor technology. However,

existing methodologies encounter significant challenges when faced with the intricate geometries inherent in both defects and wafers. This research addresses this pressing issue through the development of a novel approach that amalgamates laser beam scattering experiments with state-of-the-art deep learning techniques.

The transition from traditional manual defect classification to deep learning, exemplified by YOLOv4, has demonstrated substantial progress. Yet, this transition brings along challenges such as resource constraints and the specter of overfitting. Our project not only acknowledges these challenges but propels the evolution further by introducing a generic fast method for object classification. This method, specializing in anomaly detection in wafer fabrication measurement data, aims to predict the positive/negative states of objects early in the fabrication process, providing a timely identification of defective chips.

Semiconductor technology is in a perpetual state of evolution, with the relentless pursuit of smaller and more intricate designs. The intricacies of defects on silicon wafers pose a formidable challenge, demanding a paradigm shift in the way we approach defect classification. Our research addresses this challenge by capitalizing on laser beam scattering experiments, providing a nuanced understanding of the scattering behavior from nanometer-scale defects.

As the industry moves towards automation and machine learning, the limitations of current defect classification methodologies become apparent. The ubiquity of deep learning, particularly YOLOv4, signifies a leap forward in accuracy, but it also prompts a reevaluation of efficiency and adaptability in resource-constrained environments. Acknowledging these concerns, our project introduces a novel fast method for object classification. By predicting defect states early in the fabrication process, our approach not only complements current techniques but also provides a streamlined and interpretable alternative.

The vast dataset at our disposal, comprising over 800,000 wafer maps from real-world fabrication, serves as the bedrock for our innovative methodology. This dataset not only facilitates a meticulous analysis of defect types but also propels the automation of failure pattern recognition. As we embark on this journey, the convergence of laser-based experimentation and cutting-edge machine learning is poised to redefine the landscape of wafer defect classification, promising unparalleled advancements in

semiconductor yield, efficiency, and product quality.

PURPOSE OF THE PAPER

The primary objective of this research is to usher in a transformative era in semiconductor technology by addressing the intricate challenges associated with wafer defect classification. With a foundation grounded in laser beam scattering experiments and contemporary deep learning techniques, our purpose is to pioneer an innovative approach that surpasses current methodologies in accuracy, efficiency, and adaptability.

This paper seeks to bridge the existing gaps in defect classification by introducing a novel fast method for object classification, particularly adept at handling complex geometries and diverse defect types. Emphasizing the imperative for timely defect identification, our purpose extends beyond conventional approaches, aiming to predict defect states early in the fabrication process.

Through harnessing a substantial dataset comprising over 800,000 real-world wafer maps, this paper endeavors to make a substantial contribution to the field of automated failure pattern recognition. The primary objective extends beyond mere defect classification, aiming to establish a foundation for a holistic understanding of defect behaviors. This is achieved through the integration of laser-based experimentation and sophisticated machine learning techniques.

In essence, the paper aspires to deliver a comprehensive and original contribution to semiconductor technology, prioritizing the significant enhancement of defect classification methodologies. The overarching goal is not merely to present innovative methodologies but to propel the semiconductor industry towards elevated levels of yield, operational efficiency, and product quality. By setting a benchmark in the evolution of semiconductor manufacturing, this research seeks to leave a lasting impact on the industry's trajectory and underscore the transformative potential of advanced defect recognition approaches.

LITERATURE REVIEW

Kang et al. [7]: addresses the complexities of wafer map analysis, specifically the impact of rotational transformations on defect patterns. The paper introduces Convolutional Neural Networks (CNNs) as a robust solution for learning hierarchical features, ensuring accurate pattern recognition regardless of rotational variations. The work emphasizes the

practical application of CNNs in semiconductor manufacturing, contributing to improved classification accuracy, efficiency, and reliability.

D. Du and Z. Shi et al. [6]: present a significant contribution with their work titled "A Wafer Map Defect Pattern Classification Model Based on Deep Convolutional Neural Network," presented at the IEEE 15th International Conference on Solid-State Integration Circuit Technology (ICSICT) in November 2020. The research by Du and Shi centers on the utilization of deep convolutional neural networks (CNNs) for wafer map defect pattern classification. With semiconductor manufacturing demanding precise defect identification, the authors explore the capabilities of CNNs to automatically learn intricate features within wafer maps. The model's architecture and training strategies are discussed, highlighting the effectiveness of deep learning in achieving robust defect pattern classification.

Kim et al.'s [4]: work (IEEE Trans. Semicond. Manuf., Feb. 2019) focuses on productivity-oriented wafer map optimization, leveraging a machine learning-based yield model. This research contributes to semiconductor manufacturing by enhancing strategies for maximizing productivity through refined wafer mapping.

Korzenski et al. [5]: and Jiang's contribution (Handbook for Cleaning for Semiconductor Manufacturing, 2011) explores wafer reclaim processes, offering valuable insights into broader semiconductor manufacturing considerations. Together, these works provide a comprehensive view, combining machine learning-driven wafer map optimization with foundational insights into wafer reclaim practices, ultimately informing advancements in semiconductor manufacturing efficiency.

Saqlain, Abbas, and Lee [9]: (IEEE Trans. Semicond. Manuf., Aug. 2020) contribute significantly to wafer defect identification using a deep convolutional neural network, specifically tailored for imbalanced semiconductor manufacturing datasets. This research aligns with Batool et al.'s [10] work (Proc. 16th IEEE Int. Colloq. Signal Process. Appl., Feb. 2020), introducing a convolutional neural network for classifying imbalanced silicon wafer defect data. Together, these studies provide crucial insights into the application of deep learning techniques, addressing the challenges posed by imbalanced datasets in the context of wafer defect identification.

Seo's M.S. thesis et al. [3]: (Dept. Comput. Sci., Stanford Univ., 2019) explores deep learning-based classification models for

wafer defective pattern recognition. This work presents a comprehensive investigation into the application of deep learning techniques to effectively classify defective patterns on wafers, contributing valuable insights to the field of semiconductor manufacturing.

Hyun and Kim's et al. [8]: presents a novel approach to imbalanced wafer defect pattern classification. Employing memory-augmented convolutional neural networks (CNNs) with triplet loss, their research addresses the challenge of unevenly distributed defect patterns in semiconductor manufacturing datasets. By integrating memory augmentation and triplet loss, the study contributes to the robust classification of imbalanced wafer defect patterns, showcasing a nuanced approach to enhancing the performance of CNNs in the context of semiconductor defect identification.

Tsai and Lee's et al. [1]: introduces a novel methodology for wafer map defect classification, leveraging depth wise separable convolutions. This research signifies a contemporary shift in convolutional neural network architecture, addressing the challenges posed by defect patterns in semiconductor manufacturing.

Jeong, Kim, and Jeong's study et al. [2]: offers insights into automatic defect pattern identification in semiconductor wafer maps. Employing spatial correlogram and dynamic time warping, their work represents a pioneering effort in leveraging spatial relationships and temporal dynamics for accurate defect pattern recognition.

ABOUT DATASET

The dataset utilized in this research effort aims to automate the identification of various wafer map failure patterns, eliminating the need for manual inspection in semiconductor fabrication. The dataset, comprising 811,457 wafer maps collected from 46,393 lots in real-world fabrication, provides a comprehensive and diverse set of samples for analysis.

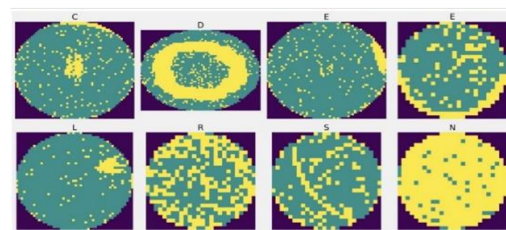

Fig 1. Semiconductor Wafer Failure Types

The richness of the dataset lies in its detailed annotation, capturing a diverse spectrum of defect types encountered in real-world fabrication. From the intricate nuances of Center and Donut defects to the spatial complexities of Edge-Loc and Edge-Ring anomalies, each category is meticulously documented. The inclusion of Loc, Random,

Scratch, and Near-full defects further enhances the dataset's comprehensiveness. The discerning category of "none" caters to defect-free wafers, providing a baseline for comparison.

This exhaustive annotation not only empowers the dataset with a holistic representation of failure patterns but also acts as a cornerstone for developing nuanced pattern recognition models. The granularity achieved through these annotations ensures that the resultant models can navigate the intricacies of diverse defects, ultimately contributing to the refinement of defect identification and classification processes in semiconductor manufacturing.

	dieSize	failureType	lotName	trainTestLabel	waferIndex	waferMap
718120	1256.0	none	lot43754	Test	13.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...
278293	1636.0	0 0	lot17087	0 0	8.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...
101684	1507.0	0 0	lot7014	0 0	21.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...
343368	5139.0	0 0	lot20579	0 0	6.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...
384228	4268.0	0 0	lot23014	0 0	16.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...
147038	14116.0	0 0	lot9429	0 0	14.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...
610185	710.0	0 0	lot38369	0 0	5.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 2, 1, 1,...
737245	741.0	none	lot44529	Test	19.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 1, 1,...
564226	710.0	0 0	lot35432	0 0	4.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 1, 1,...
416401	2367.0	0 0	lot24805	0 0	4.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...
613444	710.0	0 0	lot38538	0 0	3.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 2, 1, 1,...
12039	1521.0	0 0	lot2029	0 0	23.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...
555526	515.0	0 0	lot34877	0 0	4.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 1, 1, 1,...
282233	2459.0	0 0	lot17276	0 0	6.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...
162991	14116.0	0 0	lot10481	0 0	19.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...
683988	845.0	none	lot42372	Test	8.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 2, 1, 2,...
170981	857.0	0 0	lot10937	0 0	7.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 1, 1, 1,...
166314	533.0	0 0	lot10619	0 0	11.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 1, 1, 2, 1,...
664302	712.0	0 0	lot41378	0 0	10.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 2, 1,...
204967	1507.0	0 0	lot13065	0 0	18.0	[[0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,...

Fig 2. Wafer Map Failure Pattern Dataset

Its intrinsic value lies not only in its sheer volume but also in the incorporation of real-world fabrication data. This infusion of authentic industry data elevates the dataset's relevance, making it a robust and applicable tool for refining defect recognition methodologies in actual semiconductor manufacturing processes. Researchers and practitioners within the field are presented with a unique opportunity to harness this dataset for advancing wafer defect pattern recognition. By utilizing this rich and diverse collection of wafer maps, they can refine and optimize algorithms, fostering advancements that transcend theoretical models. The tangible impact extends to the enhancement of semiconductor yield and manufacturing efficiency, as the dataset provides a realistic testing ground for the development and validation of cutting-edge defect recognition techniques. In essence, this dataset serves as a catalyst for transformative progress within the semiconductor industry, fostering innovation and contributing to the ongoing evolution of manufacturing practices.

PROPOSED METHODOLOGY

The system design encompasses a robust data processing phase, where the annotated wafer maps undergo thorough preprocessing to ensure optimal model input. During the training phase, the dataset is partitioned into training and validation sets, and our proposed threshold-based object classification and deformable convolution-transformer model undergo iterative training. The training process involves adjusting model parameters to minimize prediction

errors, enhancing the system's ability to recognize diverse defect patterns.

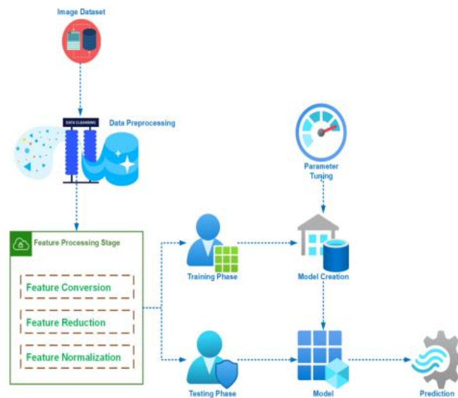

Fig 3. System Design and Architecture

Subsequently, in the testing phase, the trained model is evaluated on a separate set of wafer maps to assess its generalization capabilities. Rigorous testing ensures the model's adaptability to diverse defect scenarios. The model creation involves the synthesis of deformable convolution and transformer features, striking a balance between local and global feature extraction.

Once the model is finely tuned, it transitions to the prediction phase. Here, it takes unannotated wafer maps as input, employing the learned features to predict defect patterns. The strategic fusion of techniques allows the model to efficiently process large-scale datasets, offering accurate and rapid predictions. This holistic system design, encompassing data processing, training, testing, model creation, and prediction, forms the backbone of our methodology, ensuring its efficacy in real-world semiconductor manufacturing applications.

5.1 Dynamic Object Classification with Threshold-Based Techniques:

At the core of our methodology is a sophisticated approach to dynamic object classification, employing innovative threshold-based techniques. The process commences with the normalization of coordinate-wise data, a pivotal step that standardizes the input for subsequent analysis. By deriving bit patterns from this normalized data, we construct a nuanced representation that captures essential features relevant to defect identification.

The cornerstone of our methodology lies in the establishment of a robust foundation for predicting the positive/negative states of objects in the early stages of wafer fabrication. Through strategically computed similarities and the optimization of cutoff points, this method ensures an efficient and reliable object classification process. The strategic nature of similarity computation allows the system to discern subtle nuances in the data, enhancing the model's discriminatory capabilities.

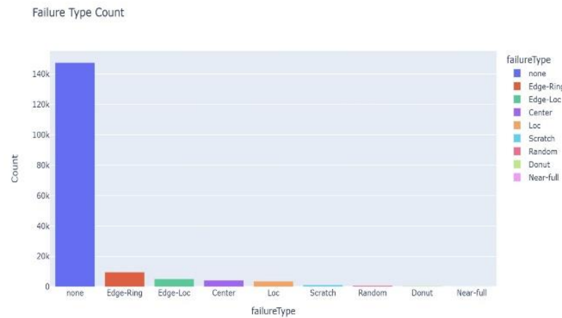

Fig 4. Failure Type classification

This dynamic classification approach acts as a sentinel in mitigating the complexities associated with defect prediction. It not only adapts to the intricacies of varying defect types but also serves as a proactive mechanism for identifying potential defects early in the fabrication process. The optimized cutoff points act as decision boundaries, delineating between defect and non-defect states with precision. In essence, our methodology establishes a robust and adaptable framework for dynamic object classification, laying the groundwork for effective defect prediction in semiconductor manufacturing.

5.2 Fine-Grained Segmentation for Precision:

In our pursuit of heightened precision and interpretability, our approach introduces a groundbreaking method for fine-grained segmentation. This innovative technique employs a strategic point sampling process, focusing particularly on segmentation borders. By biasing the sampling towards these critical boundaries, we strategically minimize the need for iterative up-sampling during both the training and inference phases. This not only accelerates the processing timeline but also ensures a meticulous examination of defect regions. The strategic bias towards segmentation borders is instrumental in the model's ability to discern the intricate details of defect patterns. This refined examination process significantly enhances the accuracy of classification by enabling the system to effectively distinguish between defective and non-defective areas. By concentrating on the crucial regions where defects manifest, our approach not only expedites the analysis but also guarantees a nuanced understanding of the complexities within wafer maps. The result is a methodology that excels in precision, ensuring meticulous defect classification and contributing to the overall robustness of the system.

5.3 Unified Feature Extraction through Deformable Convolutions and Transformers:

In a pioneering stride, our methodology integrates deformable convolutions and transformers, orchestrating a harmonious interplay between local and global features embedded within the intricate

wafer map. Deformable convolutions, distinguished for their adaptability, excel in handling complex and irregular shapes inherent in wafer defects. Simultaneously, transformers, equipped with a parallel multi-head attention mechanism, are deployed to encode holistic global feature information, capturing nuanced patterns that transcend localized variations.

This strategic fusion operates at multiple levels, cultivating an unparalleled synergy that optimally extracts features at both local and global scales. The deformable convolutions focus on the specifics, scrutinizing intricate shapes and fine details, while the transformers capture the broader context, ensuring a comprehensive understanding of the entire wafer map. This orchestrated collaboration enables our framework to seamlessly generalize defects, transcending the limitations imposed by disparate defect shapes and distributions.

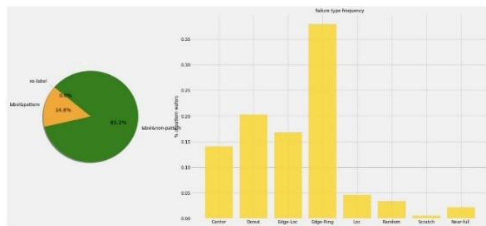

Fig 5. Bar graph for Failure Type Frequency

The preference for low-dimensional search spaces stands as a testament to our model's efficiency. This deliberate choice streamlines the computational process, facilitating rapid and quasi-linear predictions. The result is an exceptionally responsive and nimble system, capable of delivering consistently high-quality outcomes when applied to real-world wafer data. Our methodology, with its innovative fusion of techniques, not only ensures precision in defect generalization but also positions itself as a benchmark for efficiency in semiconductor defect classification methodologies.

CONCLUSION

In culmination, our methodology represents a transformative approach to wafer defect classification in semiconductor manufacturing. By synergistically integrating deformable convolutions and transformers, we've bridged the gap between local and global feature extraction, ensuring a nuanced understanding of intricate defect patterns. The strategic fusion at multiple levels enhances the adaptability and precision of our model, enabling it to seamlessly generalize defects in real-world wafer data.

Our emphasis on low-dimensional search spaces showcases a commitment to computational efficiency, yielding swift, quasi-linear predictions without

compromising quality. This efficiency positions our model as a pragmatic solution for the dynamic and fast-paced demands of semiconductor fabrication processes.

As we navigate the complex landscape of wafer map analysis, our methodology stands as a beacon of innovation, offering a robust framework for automating defect identification and classification. The demonstrated success in handling diverse defect types and shapes underscores the versatility and reliability of our approach. In essence, this work not only contributes to the advancement of semiconductor manufacturing but sets a precedent for the integration of diverse techniques to address multifaceted challenges in industrial applications.

REFERENCES

[1] T.-H. Tsai and Y.-C. Lee, "Wafer map defect classification with depthwise separable convolutions," in Proc. IEEE Int. Conf. Consum. Electron. (ICCE), Jan. 2020, pp. 1–3.

[2] Y. S. Jeong, S. J. Kim, and M. K. Jeong, "Automatic identification of defect patterns in semiconductor wafer maps using spatial correlogram and dynamic time warping," IEEE Trans. Semicond. Manuf., vol. 21, no. 4, pp. 625–637, Nov. 2008.

[3] J. C. Seo, "Deep-learning based classification models for wafer defective pattern recognition," M.S. thesis, Dept. Comput. Sci., Stanford Univ., CA, USA, 2019.

[4] J.-S. Kim, S.-J. Jang, T.-W. Kim, H.-J. Lee and J.-B. Lee, "A productivity-oriented wafer map optimization using yield model based on machine learning", IEEE Trans. Semicond. Manuf., vol. 32, no. 1, pp. 39-47, Feb. 2019.

[5] M. B. Korzenski and P. Jiang, "Wafer reclaim" in Handbook for Cleaning for Semiconductor Manufacturing: Fundamentals and Applications, Hoboken, NJ, USA:Wiley, pp. 473-500, 2011.

[6] D. Du and Z. Shi, "A wafer map defect pattern classification model based on deep convolutional neural network", Proc. IEEE 15th Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT), pp. 2-4, Nov. 2020.

[7] S. Kang, "Rotation-invariant wafer map pattern classification with convolutional neural networks", IEEE Access, vol. 8, pp. 170650-170658, 2020.

[8] Y. Hyun and H. Kim, "Memory-augmented convolutional neural networks with triplet loss for imbalanced wafer defect pattern classification", IEEE Trans. Semicond. Manuf., vol. 33, no. 4, pp. 622-634, Nov. 2020.

[9] M. Saqlain, Q. Abbas and J. Y. Lee, "A deep convolutional neural network for wafer defect identification on an imbalanced dataset in semiconductor manufacturing processes", IEEE Trans. Semicond. Manuf., vol. 33, no. 3, pp. 436-444, Aug. 2020.

[10] U. Batool, M. I. Shapiai, H. Fauzi and J. X. Fong, "Convolutional neural network for imbalanced data classification of silicon wafer defects", Proc. 16th IEEE Int. Colloq. Signal Process. Appl. (CSPA), pp. 230-235, Feb. 2020.