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A Capacitorless Analog Ldo For Output Adjusting The Frequency Of A Four-Stage Amplifier

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Abstract. In this paper,we implement an output-capacitorless analog low-dropout voltage regulator (ALDO) with frequency compensation of a four-stage amplifier, which consists of a pass transistor (MP) created last stage and a three-stage error amplifier (EA) without cascading. Because of the three gain stages in the EA, it achieves good output voltage regulation at low supply-voltage (Vdd) with an unsaturated MP (e.g., dropout voltage of 30 mV under 0.5 V supply). By utilizing the root-locus diagram (TFR) method in a two-port feedback analysis, which offers an intuitive comprehension of pole/zero dynamics in the s-plane, frequency compensation is accomplished. The suggested ALDO, which is made in LT spice CMOS implementation, exhibits asymptotic stability under a variety of operating conditions: Vdd of 0.5–1.8 V, capacitance of the load.

Keywords: ALDO, FPGA, Verilog HDL, Capacitors.

I.INTRODUCTION

An Analog Low-Dropout Voltage Regulator (ALDO) is a type of voltage regulator circuit used in electronic devices to provide a stable output voltage with minimal voltage dropout. Voltage regulators are crucial components in electronic systems, ensuring that the voltage supplied to sensitive components remains within specified limits, regardless of fluctuations in the input voltage or current.

The term "low-dropout" refers to the ability of the regulator to maintain a stable output voltage even when the input voltage is only slightly higher than the desired output voltage. This is particularly important in battery-powered devices or in applications where the available input voltage is close to the desired output voltage.

ALDOs are analog devices, meaning they use continuous signals to control the output voltage. They typically consist of a pass transistor, a voltage reference, an error amplifier, and feedback circuitry. Here's a brief overview of how they are working of Pass Transistor is the pass transistor is the main component responsible for regulating the output voltage. It controls the flow of current from the input to the output based on the control signal it receives. The voltage Reference is the voltage reference provides a stable reference voltage against which the output voltage is compared. This reference voltage is typically generated using precision components like zener diodes or bandgap voltage references. Error Amplifier is an error amplifier compares the actual output voltage with the desired reference voltage and generates an error signal proportional to the difference between the two. This error signal is then used to adjust the pass

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transistor to maintain the desired output voltage.

The feedback circuitry provides a means for the output voltage to be monitored and compared to the reference voltage. It adjusts the control signal sent to the pass transistor based on the error signal from the error amplifier.

The key advantage of ALDOs is their ability to regulate the output voltage with minimal dropout voltage, meaning they can maintain a stable output even when the input voltage is very close to the desired output voltage. This is achieved through careful design and optimization of the internal circuitry. ALDOs find applications in a wide range of electronic devices, including battery-powered devices, voltage-sensitive circuits, and precision instrumentation. Their ability to provide a stable and regulated output voltage makes them essential components in modern electronic systems.

Digital low-dropout regulators (LDOs) have achieved much attention in the recent past due to low supplyvoltage (Vdd) [1], [2], [3]. However, they suffer from output ripple and poor power-supply-rejection (PSR). By contrast, analog LDO [4], [5], [6] (ALDO) is free from the ripple and has better PSR if a loop-gain of the ALDO is large enough. unfortunately, to achieve the large loop-gain, ALDOs typically require high Vdd as the pass transistor (MP) should be saturated (i.e., pinch-offed with $V_{SD} > V_{SG} - |V_{TH}|$ in MP, where V_{SD}, V_{SG}, and V_{TH} are source-to-drain, source-to-gate, and threshold voltage of MOSFET). Though an ALDO that has

a very small dropout voltage of 50 mV with unsaturated MP was recently proposed in [7], it requires a minimum Vdd of 0.9 V due to four-stacked transistors. Also, it exhibits a poor low-frequency PSR of about −30 dB because of the small dc loop-gain of about 40 dB provided only by a single-stage gain-boosted amplifier.

To achieve both the low-supply operation and large loopgain, a design of ALDO based on a multi-stage error amplifier (EA) that does not use cascoding can be an attractive solution.For example, if the EA has three gain stages, it can provide a large loop-gain even with unsaturated MP under ultra-low Vdd,thus achieving a good low-frequency PSR. Unfortunately, such ALDO has four low-frequency poles when the load current is small, requiring sophisticated frequency compensation. While previous works have relied on direct analysis [6], [8] (i.e., solving node equations to achieve the desired transfer function), it is extremely difficult and complex that design intuition cannot be obtained.

Alternatively, a two-port feedback analysis together with a root-locus diagram (TFR) method [9], [10] can be useful in compensating such a multi-stage-EA-based ALDO because the root-locus diagram provides a designer with an intuitive understanding for pole/zero dynamics in the s-plane, which can be translated to simulation results much better than the direct analysis and provide design intuition.

This project is an output-capacitorless ALDO featuring frequency compensation of a four-stage amplifier consisting of a three-stage EA that does not use cascoding, plus a last stage formed by MP, where the frequency compensation is achieved by the TFR method. Regardless of the operating condtions,the proposed ALDO always behaves as a single-pole

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system, thus achieving the stability. Fabricated in 0.18 μm CMOS, it achieves asymptotic stability over a wide range of operating conditions: Vdd of 0.5∼1.8 V, load capacitance (CL) of 0∼50 pF, load current (IL) of 0∼2 mA (0∼200 mA) under Vdd of 0.5 V (1.8 V) and temperature of −20∼125 ◦C. Also, it does not require minimum on-chip output capacitance for loop stabilization, thus achieving a small area of 0.0035 mm2 with a state-of-the-art current density of 11.4 A/mm2. Moreover, it achieves a good low-frequency PSR of −62 dB (−47 dB) when IL = 0 mA (2 mA) under Vdd of 0.5 V and the dropout voltage of 30 mV, consuming of only 11 μW.

II. PROPOSED METHOD AND ITS METHODOLOGY

This project proposes an output-capacitorless ALDO featuring frequency compensation of a four-stage amplifier consisting of a three-stage EA plus the last stage formed by MP. Stability analysis is analyzed using the TFR method, based on which we were able to design and optimize the proposed ALDO. The resulting frequency compensation scheme guarantees stability over a wide range of operating conditions. Simulated in LT Spice analysis of CMOS, the proposed ALDO achieves stability over the supply voltage of 0.5∼1.8 V, load capacitance of 0∼50 pF, load current of 0∼200 mA, and temperature of −20∼125 ◦C. Specifically, it does not require minimum on-chip output capacitance, thus achieving a small area of 0.0035 mm2, which results in state-of-the-art current density of 11.4 A/mm2. Also, the excellent low-frequency PSR of −62 dB even under low supply-voltage with an unsaturated MP (e.g., VD D = 0.5 V, Vout = 0.47 V with the dropout voltage of only 30 mV) is achieved because the EA still has three remaining gain stages that provide the large dc loop transmission magnitude without stability problems.

The transistor-level implementation in a standard LT-SPICE SIMULATOR WITH BSIM CMOS with the value of bias current in each branch is shown in Fig. 1. The device sizes and their associated transconductance are shown in Table I. All transistors in the EA are low threshold devices (|VT H | 260 mV for both n/pMOS) and operate in the saturation region except for the input nMOS-pair M0L,R which is a nominal device (VT H 540 mV) that operates in the sub-threshold region. Using the nominal threshold device allows large width to minimize both the output offset voltage and 1/f noise. Also since there is no cascoding, it can operate under Vdd down to 0.5 V. All devices have a minimum channel length that provides high transconductance for a given bias current except for the tail current source MB in the differential first stage. MB is biased with a current of 3 μA, allowing M1L to be biased with a current of 1.5 μA that is sufficient to push a mirror pole associated with v0 node a high frequency.

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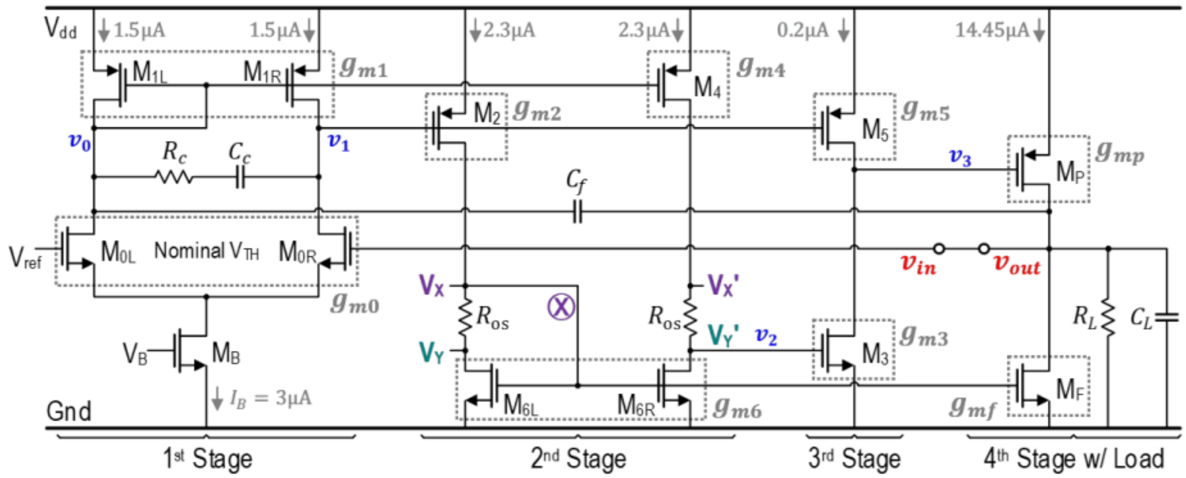

Fig1. CMOS Implementation of ALDO.

The equivalent block diagram is shown in Fig. 5 with acouple of modifications from the block diagram in Fig. 1. 1) The ALDO core in the top-solid box is slightly modified to include the gate node of M6L , M6R, and MF (i.e., a node annotated with X) in the forward signal path. Thus, a mirror pole associated with this node should be located at high frequency to be neglected similar to the pole at v0 node; otherwise, the additional pole can cause the loci to deviate from the ones in Fig. 3. In our design, this is achieved by setting a large gm6 with a sufficient dc bias current of 2.3 µA and a small lumped capacitance at this node by having small widths for M6L , M6R, and MF . However, this causes asymmetric size-ratio between the second stage and third stage in the EA, which results in the systematic output offset voltage; note that the pMOS size ratio between M2 : M5 = 12 : 1 is not preserved in the nMOS size ratio M6L : M3 = 1 : 1 in Table I. To mitigate this problem, two high-poly resistors Ros (40 kOHMS) are added to equalize dc voltages at the drain of M2 and M4 and equalize dc voltages at the drain of M6L and M6R (i.e., VX =VX' and VY = VY' in Fig. 1).

2) The transconductance of gm0/2, gm4, and gm5 are added as shown in the bottom-dotted box. This is because gm0 is split into half to model the differential input-pair and that gm4, gm5,which are transconductances of M4 and M5 respectively, are added as a result of connecting the gate of M4 and M5 to the v0 and v1 node, respectively. Thus, they may modify L(s);however, such modification3 does not significantly change the fact that the ALDO has a single-pole behavior as we will see in transistor-level simulation results. Note that large-signal responses such as load transient and reference tracking are improved by them as they serve as internal push-pull stages for class AB behavior at the three gain-nodes (v1−3). Moreover, such connections reduce the number of additional current bias sources since all quiescent operating currents in the EA are referenced to the bias current IB of the differential first-stage.

In this section, we compare the load regulation accuracy under two-, three-, and four-stage regulations by connecting the gate of the MP to v1, v2, and v3 nodes in Fig. 4 without hanging any sizes of the devices, respectively. Note that in the two

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former cases Vref and Vout positions are changed. Under the operating condtion that Vdd = 0.5 V and Vref = 0.47 V, the simulated load regulations are shown in Fig. 6. The dc loop transmission magnitude and load regulation are 19.2 dB and 15.8 mV/mA, 45.3 dB and 1.4 mV/mA, and 71 dB and 0.047 mV/mA, under the two-, three, and four-stage regulation, respectively. Obviously, the proposed ALDO has a good load regulation due to enhanced loop-gain.

III. RESULTS AND ANALYSIS DISCUSSION

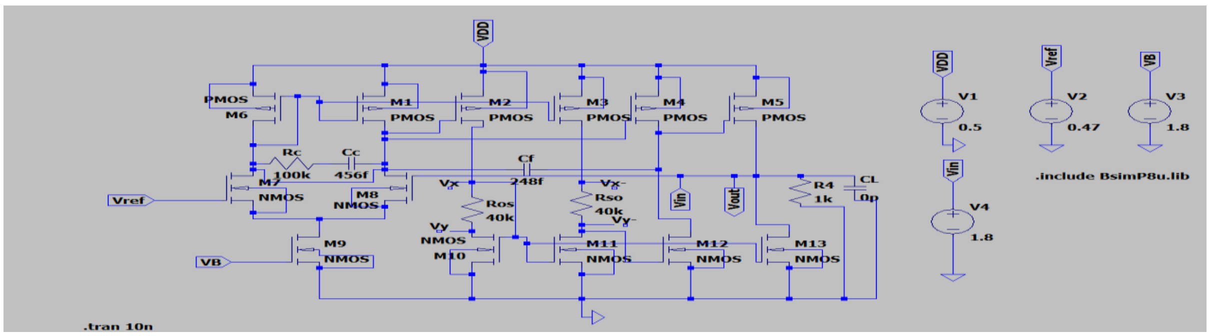

Fig1.Simulated ALDO CMOS Implementation circuit diagram

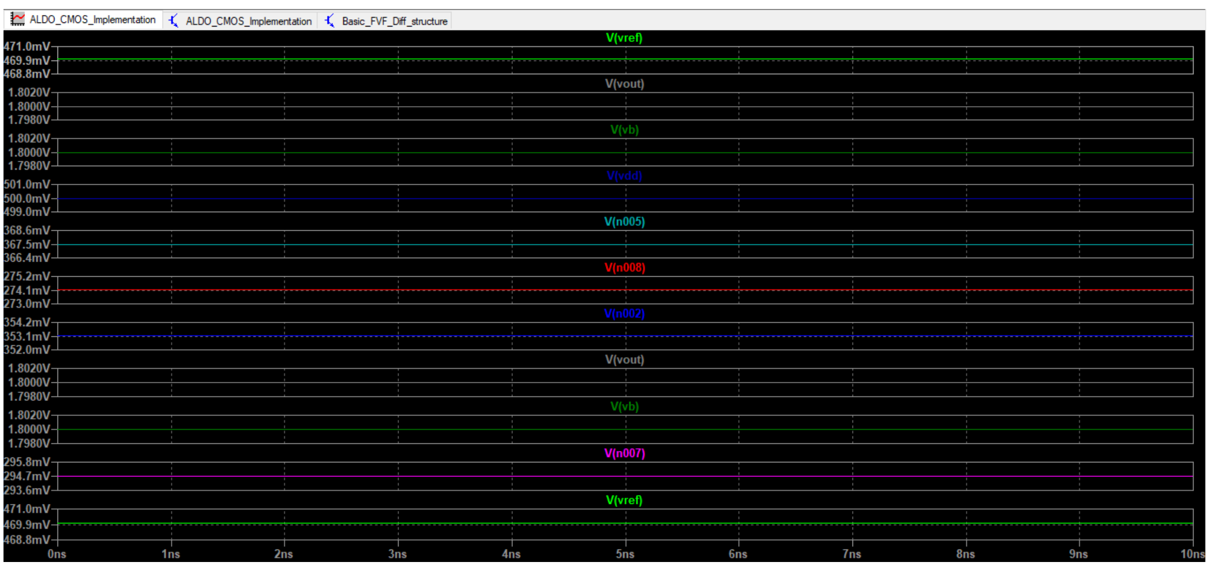

Fig2.output of ALDO CMOS.

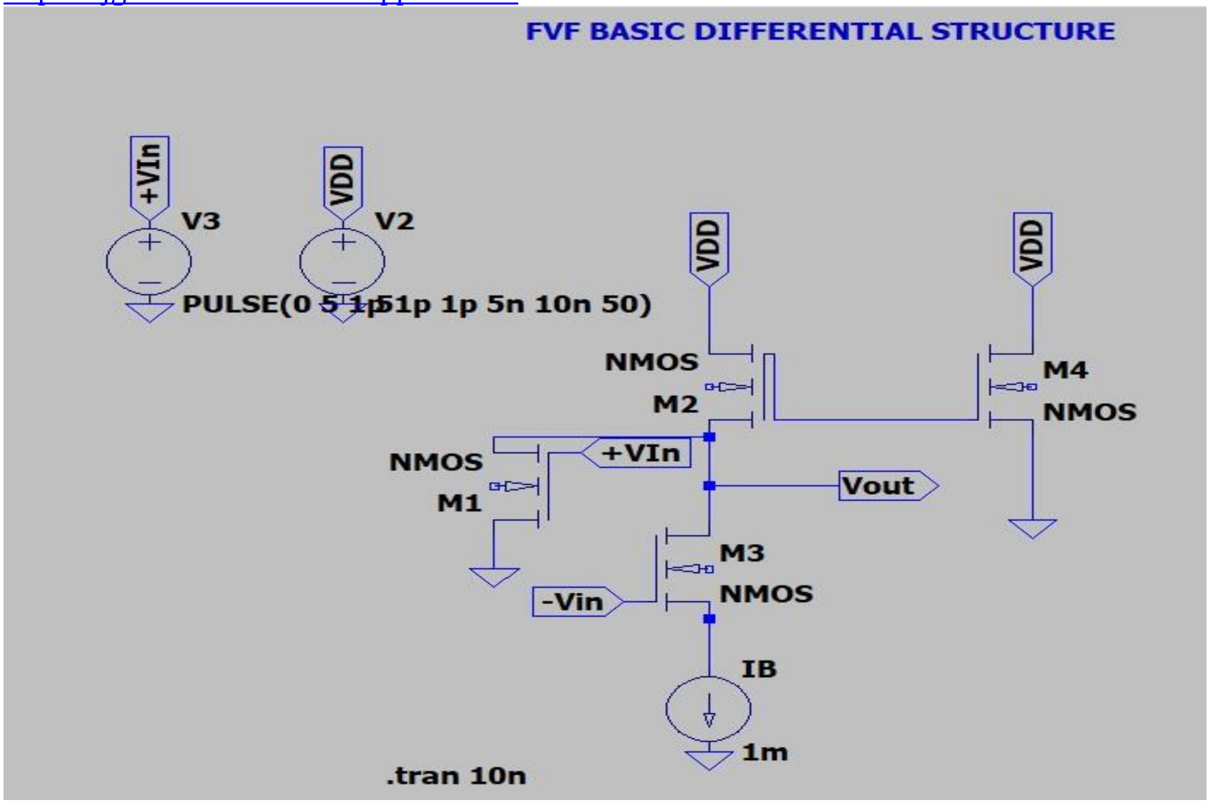

Fig3.FVF simulated circuit diagram

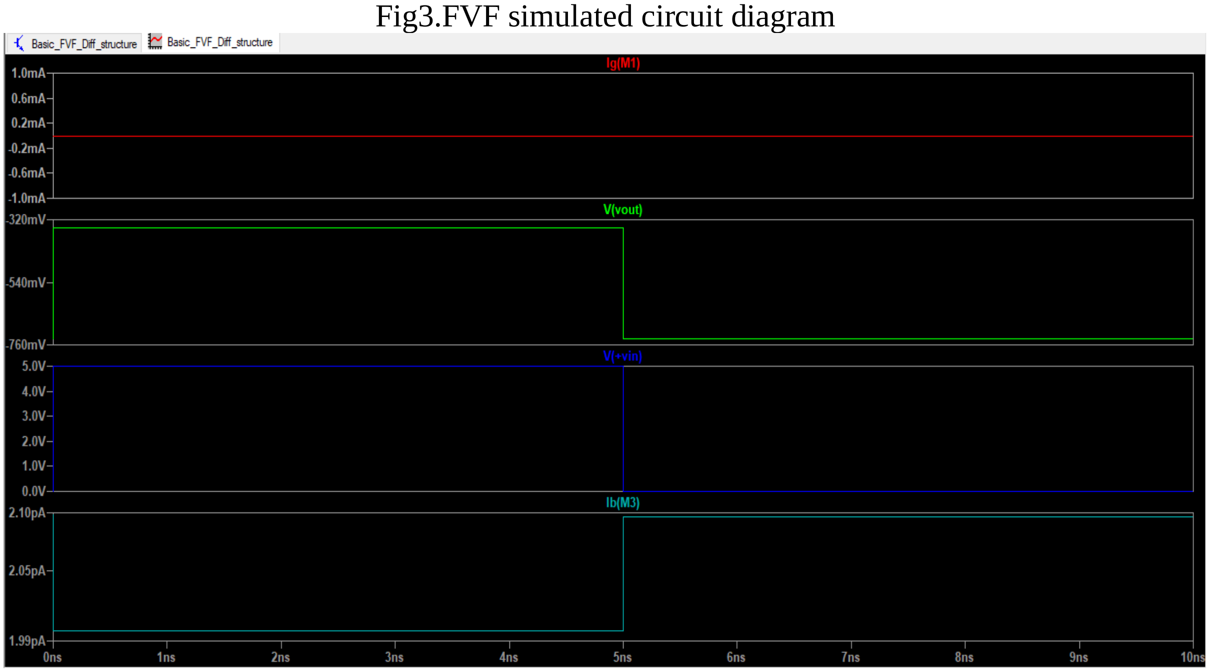

Fig4.FVF simulated output

CONCLUSION

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This paper, This paper proposes an output-capacitorless ALDO featuring frequency compensation of a four-stage amplifier consisting of a three-stage EA plus the last stage formed by MP . Stability analysis is analyzed using the TFR method, based on which we were able to design and optimize the proposed ALDO. The resulting frequency compensation scheme guarantees stability over a wide range of operating conditions. Fabricated in 0.18 μm CMOS, the proposed ALDO achieves stability over the supply voltage of 0.5∼1.8V, load capacitance of 0∼50 pF, load current of 0∼200 mA, and temperature of −20∼125 ◦C.

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