COARSE-GRAIN POWER GATING TECHNIQUE FOR CLOCK PAIR SHARED FLIP FLOP FOR LOW POWER AND HIGH SPEED CLOCK DISTRIBUTION

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Abstract*—The power savings is maximized by creating a high-fanout physically or electrically symmetric distribution that feeds many CM flip-flop (FF) receivers. Logic signals the FF receivers retain VM compatibility with low-power CMOS logic in the remainder of the chip. This paper presents the first true CM CDN and a new CM pulsed D-type FF where the clock (CLK) input is a CM receiver and the data input (D), an active low enable ,and output (Q) are VM.A new paradigm for clock distribution that uses current, rather than voltage, to distribute a global clock signal with reduced power consumption. While current-mode (CM) signaling has been used in one-to-one signals, this is the first usage in a one-to-many clock distribution network. To accomplish this, a new high-performance current-mode pulsed flip-flop with enable (CMPFFE) using 45 nm CMOS technology. When the CMPFFE is combined with a CM transmitter, the first CM clock distribution network exhibits 62% lower average power compared to traditional voltage mode clocks. Transistor-based power-gating is implemented by placing sleep transistors in-line between the circuit and the power network or the ground network.*

Keywords—Clock distribution network, crosstalk, current-mode, flip-flop, low-power, power gating

1. INTRODUCTION

2. Long battery life durations are required for portable electronic devices, which can only be achieved by using low-power components. As connection in scaled technologies consumes a growing amount of power, low-power design has recently become extremely crucial in synchronous application specific integrated circuits (ASICs) and system-on-chips (SOCs). Researchers have shown that global buses, clock distribution networks (CDNs), and synchronous signals in general are the main users of this electricity. For instance, the CDN in the POWER4 CPU wastes 70% of the overall chip power. Interconnect latency, in addition to electricity, is a significant barrier to high-frequency operation. While increasing global interconnect time, technology scaling decreases transistor and local interconnect delay. Furthermore, due to the fact that skew, jitter, and variability are often inversely related to huge latencies, standard CDN topologies are becoming more and more challenging for multi-GHz ICs. Current-mode (CM) logic was a desirable high-speed signaling system prior to and in early CMOS technology. To achieve these fast speeds, CM logic requires a large amount of static electricity, however. Because of this, the de facto standard logic family for many years has been CMOS standard voltage-mode (VM) signaling. However, there are several very appealing methods to assist solve the interconnect power and variability issues, including low-swing and current-mode signaling.

3. In a CM signaling architecture, static power often outweighs dynamic power use. However, the static power is often substantially lower than the dynamic power of VM, and the global CM connection has significantly lower latency than VM. Due to the lack of buffers with source/drain diffusion zones that may be struck by high-energy particles, CM signaling methods also provide improved dependability since they are less vulnerable to single-event transient upsets. Prior CM techniques have been used to frequently occurring off-chip signals. However, standard logic signals have stayed VM in order to take use of CMOS logic's low static power.

4. Leakage power has grown to be a serious issue in contemporary low-power microprocessors as transistor sizes shrink and degrees of integration rise. This is particularly true for ultra-low-voltage (ULV) circuits, where high leakage levels compel designers to choose relatively high threshold voltages, limiting performance. In this thesis, the widely utilized power-gating technique—in which transistors are employed to cut off power to inactive parts of a chip—is investigated. Current power-gating implementations suffer from drawbacks including non-zero state leakage, which may add up to a lot of energy lost over extended periods of inactivity, and significant energy overhead, which restricts its applicability to protracted system-wide sleep modes. However, as this thesis will demonstrate, leakage in microprocessors may be substantially reduced by using upcoming technologies to greatly increase power-gating's efficacy and by enacting strong hardware-oriented power-gating policies. Due to the ability to reduce the threshold voltage, ULV microprocessors with great performance and low switching energy are produced.

5. EASE OF USE

A. Literature review

The Literature [1] reviews a number of low swing on- chip interconnect schemes and presents a thorogh analysis of their effectiveness and limitations.The performance of each of the presented circuits is thoroughly examined using simulation on a

benchmark interconnect circuit. The Literature [2] reviews the fourth generation power processorchip contains 170M transistors and includes 2 microprocessor cores.It is implemented in a 0.18/spl mu/m SOI technology, with 7 layers of Cu interconnect, and functions in systems at 1.1 GHz and dissipates 115W at 1.5V. The literature [3] reviews the characterization of on- chip interconnect is considered with particular attention to ultrasmall capacitance measurement and in-suit noise evaluation techniques. An approach to measuring femto- Farad level wiring capacitance is presented that is based on the concept of supplying and removing charge with active devices.The Literature [4] reviews the global wire delay becomes a major bottleneck in realizing high performance SOCs.Apart from the tecnological efforts being made to overcome the problem.It is necessary to develop new circuitdesign techniques. The Literature [5] reviews the high performance clock distribution has been a challenge for nearly three decades. This provides a thorough discussion ofcurrent issues in clock synthesis and conclude with insight into future research and design challenges for the community at large.

B. Scope of this Paper

It is not practical to make each individual point-to-pointsegment of the CDN CM, but the clock signal should still benefit from the power and reliability of CM signaling. Instead, the power savings is maximized by creating a high-fanout physically or electrically symmetric distribution that feeds many CM flip-flop (FF) receivers. Logic signals the FF receivers retain VM compatibility with low-power CMOS logic in the remainder of the chip. This project, present the first true CM CDN and a new CM pulsed D-typeFF where the clock (CLK) input is a CM receiver and the data input (D), an active low enable ,andoutput (Q) are VM.

6. LOW POWER CLOCK DISTRIBUTION USING CURRENT PULSED CLOCKED FF WITH ENABLE

However, there are several very appealing methods to assist solve the interconnect power and variability issues, including low-swing and current-mode signaling. In a CM signaling architecture, static power often outweighs dynamic power use. However, the static power is often substantially lower than the dynamic power of VM, and the global CM connection has significantly lower latency than VM. Because there aren't any buffers with source/drain diffusion zones that may be struck by high-energy particles, CM signaling methods also have improved dependability because they are less vulnerable to single-event transient upsets. Prior CM techniques have been used to frequently occurring off-chip signals. However, standard logic signals have stayed VM in order to take use of CMOS logic's low static power.

Although it is impractical in this approach to make each individual point-to-point CDN segment CM, the clock signal should nevertheless gain from the strength and dependability of CM signaling. Instead, a high-fanout, physically or electrically symmetric distribution that supplies several CM flip-flop (FF) receivers maximizes power savings. The low-power CMOS logic in the rest of the device is still VM compatible with the logic signals on the FF receivers. In a CM signaling system, a transmitter (Tx) uses a VM input signal to send a current into an interconnect (transmission line) with a small voltage swing, while a receiver (Rx) transforms current to voltage and outputs a full swing voltage. A CMOS inverter is used as the Tx in the representative CM scheme, while a transimpedance amplifier serves as the basis for the Rx.

A. Previous CM Signaling scheme

In a CM signaling scheme, a transmitter (Tx) utilizes a VM input signal to transmit a current with minimal voltage swing into an interconnect (transmission line), while a receiver (Rx) converts current-to-voltage providing a full swing output voltage. The representative CM scheme uses a CMOS inverter as the Tx while the Rx is based on a transimpedance amplifier. This scheme provides delay improvement over VM schemes, but the Rx voltage swings would cause a large CDN skew. Other researchers have used a dynamic over-driving Tx with a strong and weak driver alongside a low-gain inverter amplifier Rx and a controlled current source that addresses the previous problem. However, this scheme results in rise- and fall-time mismatch at the output which can be problematic in CDNs. Variation-tolerantCMsignaling schemes have used a CM Tx with corner-aware bias circuitry.

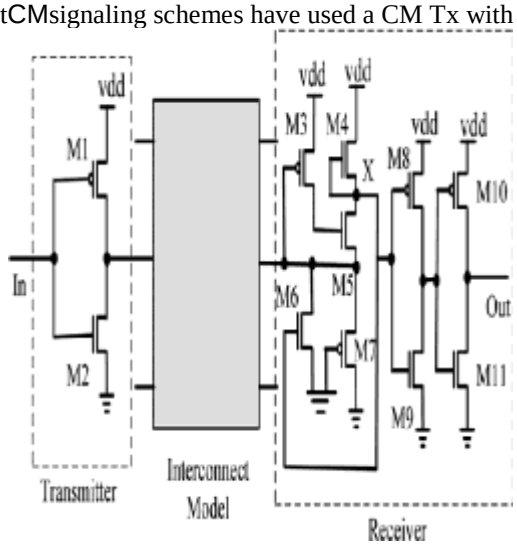


Fig. 1.Previous CM schemes used an expensive transimpedance amp Rxwhich could result in significant skew due to shift if applied to CDNs

Figure 1 depicts the variation-tolerant CM architecture with Rx and Tx circuits. In this method, the terminal point is held near the switching threshold by the inverter amplifier Rx circuit, which offers low-impedance to ground. This makes it less desirable compared to current VM signaling since it requires more static and dynamic power than the other CM approaches. For the input gate voltage of M4, a local or global reference voltage generator may be used. The robustness may be improved by using a global reference since it decreases transistor mismatch between FFs. Therefore, while integrating the CMPFFE with the CM CDN, a global reference voltage generator that diffused throughout the whole chip was employed. Additionally, this saves two transistors every FF and lowers static power with a hardly perceptible performance hit. as opposed to corner-aware reference voltage. Additionally, CM signaling does away with the need for CDN buffers, which significantly decreases active area and facilitates global reference routing.

But using a full-swing voltage to drive a CDN's lowest level produces a lot of dynamic power as well as a lot of buffer space to drive the clock pin capacitances. To cut down on total power consumption and silicon space, this CM scheme is tightly incorporated into the FFs that receive the CM signal directly.The CMPFFE employs an active-low enable signal instead of the CMPFF, which was previously published. A register stage, a static storage cell, and an input current-comparator (CC) stage are all used by the CMPFFE.

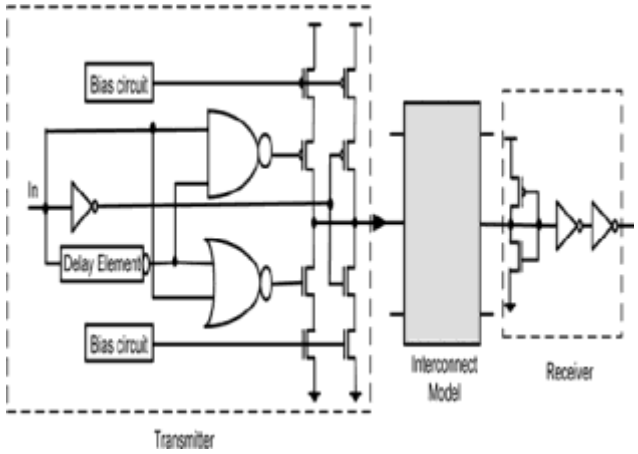


Fig. 2 Expensive variation tolerant CM signaling scheme consumes large static and dynamic power when compared to the other CM techniques.

The feedback connection from the generated voltage pulsewith M6 quickly pulls down the current comparator node B which facilitates generating a small voltage pulse and resultsin fewer transistors in the register stage. In addition, it properly size the X2 inverter so that it can efficiently drive the clock capacitance of register stage without affecting circuit performance.This comes at the expense oflarge static and dynamic power when compared to the otherCM techniques and makes it unattractive compared to existing VM signaling.This scheme results in rise- andfall-time mismatch at the output which can beproblematic in CDNs.

7. PROPOSED SYSTEM

A. Current-Mode Transmitter and Distribution

In order to integrate the CMPFFE, a Tx provides a pushpullcurrent into the clock network and distributes the required amount of current to each CMPFFE. The Tx receives a traditional voltage CLK from a PLL/clock divider at the root of the H-tree network and supplies a pulsed current to the interconnect which is held at a near constant voltage. The clock distribution is a symmetric H- tree with equal impedances in each branch so that current isdistributed equally to each CMPFFE leaf node. The NANDgate uses the CLK signal and a delayed inverted CLKsignal, clkb, as inputs to generate a small negative pulse to briefly turn on M1. Hence, the PMOS transistor briefly sources charge from the supply while the NMOS is off. Similarly, the NOR gate utilizes the negative edge of the CLK and clkb signals to briefly turn on M2. Hence, the NMOS transistor briefly sinks current while the M1 is off.

B. Power-Gating

Transistor-based power-gating is implemented by placing sleep transistors in-line between the circuit and the power network (headers) or the ground network (footers). Footers are generally more area-efficient as the high n-type mobility means less of them are needed. That being said, most commerical designs implement headers due to easier design and analysis.

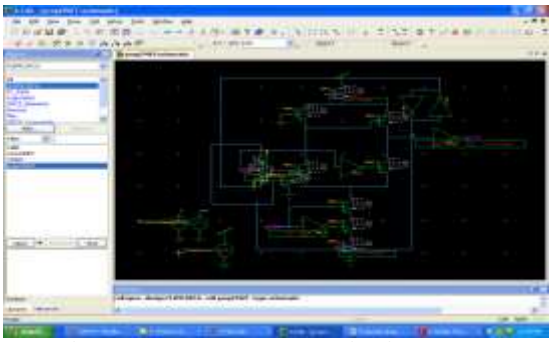


Fig. 3 Schematic of the proposed clock pair shared flip-flop using power gating technique for low power and high speed clock distribution network

especially if an external switchable voltage regulator or different power domains are used. First, the headers themselves leak, which results in a reduction but not an end to leaking. Second, the voltage drop caused by the current flowing through the headers while they are on reduces the efficiency of the power-gated circuit. With ULV processors, whose delay is exponentially dependent on supply voltage, this performance decrease is very severe; in this area, a little fluctuation in voltage results in a very huge drop in performance. The breadth of the headers controls the trade-off between state leakage reduction and latency increase. It is standard practice in the industry to design the headers such that the worst-case supply voltage loss is less than 10%, although doing so results in a significant area overhead and, typically, only achieves a 90% decrease in sleep-mode leakage. This leftover leakage might result in considerable energy loss after extended periods of inactivity. In contrast, the ultra-low power Phoenix CPU employed a limited number of footers with non-minimal channel lengths. Picowatt-range 0_-state power was produced as a consequence, although the substantial supply voltage drop only allowed for a clock frequency of 106 kHz. One of the analyses in this thesis, which uses a cutting-edge innovation called the CMOS-Compatible NEMS switch as a power-gating structure, is motivated by this trade-off and the need to significantly reduce 0_-state leakage without compromising performance.

C. Simulated Result

The clock distribution network distributes the clock signal from a common point to all the elements that need it. Since this function is vital to synchronous system, much attention has been given to the characteristics of these clock signal and the electrical networks used in their distribution. The performance of the FFs was evaluated using post-layout SPICE simulation at clock frequencies from 2–5 GHz with less than 10 psslew and a 1 V supply voltage.Figure.3 shows theSchematic of the proposed clocked pair shared flip-flop using power gating technique for low power and high speed clock distribution network. The power considers input data at 100% activity and 4 minimum size inverter load. In order to validate the functionality of the CM Tx and the proposed CMPFFE in aCDN, implemented a symmetric H-tree network spanning
1.2 mm 1.2 mm. Figure 5 Layout Design of the proposed clocked pair shared flip-flop using power gating technique for low power and high speed clock distribution network.

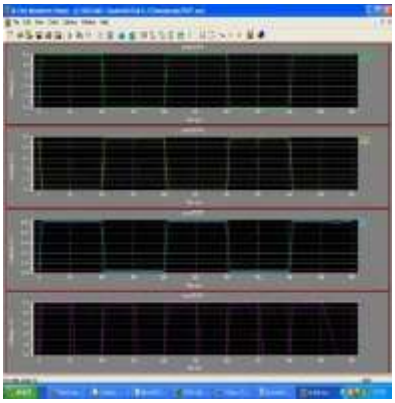


Fig. 4 Output of the proposed clock pair shared flip-flop using power gating technique for low power and high speed clock distribution network

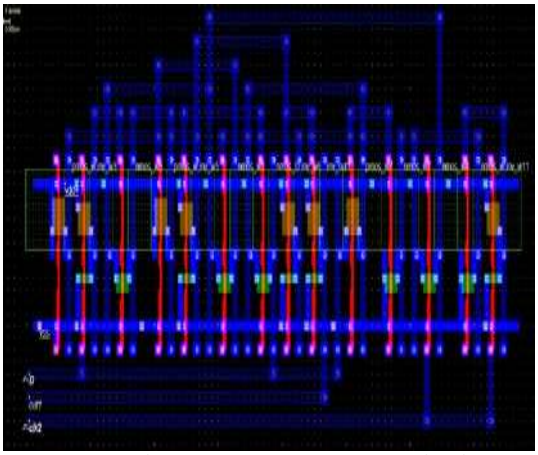
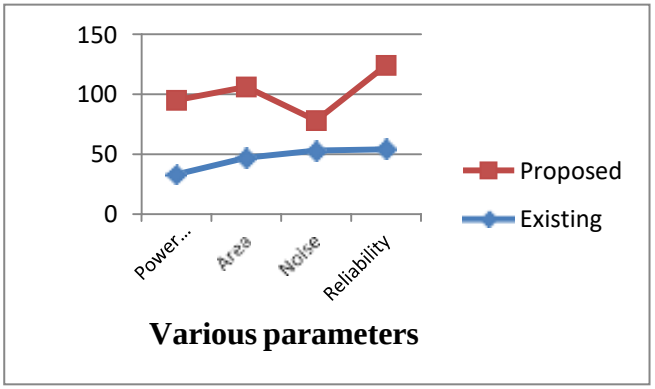
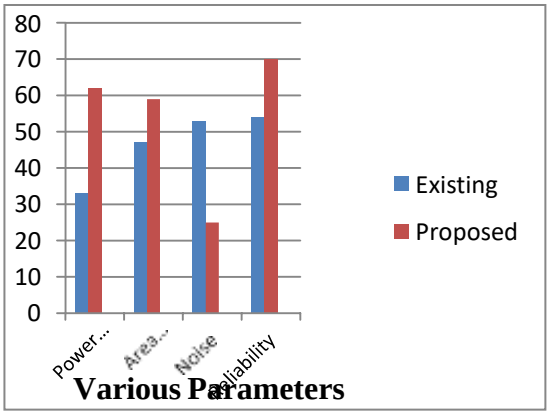


Fig. 5 Layout Design of the proposed clock pair shared flip-flop using power gating technique for low power and high speed clock distributionnetwork



(a)



(b)

Fig. 6(a) and (b)Graph comparision of Exisiting and Proposed method

8. Conclusion

In comparison to a conventional PFF at 5 GHz, the proposed Current Mode Pulsed Flip-Flop with Enable (CMPFFE) is 87% quicker, needs identical silicon area, and uses just 7% more power. Even better, when employed in a CM CDN as opposed to traditional VM CDNs, the CMPFFE offers an average power savings of 24% to 62%. Additionally, unlike other suggested CM signaling methods, the CMPFFE does not need complicated CM Rx hardware or local VM buffers to drive highly capacitive clock sinks.

Comparing the CM Clock distribution network to a voltage mode clock, the former shows lower average power. Future power reductions will be made possible by using the power gatting approach and fewer transistors, which will allow for even more layout size reduction.

Acknowledgment

The authors would like to thank each reviewer for their precious comments and suggestions and Mr.K.G.Parthiban,ASP &HoD / ECE for his support in the experiment.

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